H-bridge Gate Drive Controller

FEATURES

- Single-channel H-bridge Gate Driver
  -Drive Four External N-channel MOSFET
  -Support 100% Pulse Width Modulation (PWM) Duty Cycle
- Power Supply Range: 5.5V to 45V
- Three Control Modes:
  -PH/EN, Independent H-bridge and PWM
- Serial Interface for Configuration
- Adjustable Slew Rate Control
- Independent Control of Each H-bridge
- Support 1.8V, 3.3V and 5V Logic Inputs
- Current-shunt Amplifier
- Integrated PWM Current Regulation
- Low Power Dissipation Sleep Mode
- Protection Characteristics
  -Supply Undervoltage Lockout (UVLO)
  -Charge-pump Undervoltage (CPUV) Lockout
  -Overcurrent Protection (OCP)
  -Gate Drive Fault (GDF)
  -Thermal Shutdown (TSD)
  -Watchdog Timer
  -Fault Regulation Output(nFAULT)

APPLICATIONS

- Electric Window Regulator, Skylight, Seat, Sliding Door, Trunk and Tailgate
- Relay
- Brushed DC pumps

PRODUCT DESCRIPTION

The MS31703NA is a small single-channel H-bridge gate driver, which uses four external N-channel MOSFET to drive a bidirectional brushed DC motor.

PH/EN, independent H-bridge or PWM are allowed to be connected to the controller circuit easily. The internal sense amplifier can provide adjustable current control. And the integrated charge pumps can provide 100% duty cycle as well as driving external reverse battery switch.

The independent H-bridge mode supports H-bridge sharing and controls several DC motors. The MS31703NA has the built-in circuit, which uses the PWM current chopping with fixed off-time to adjust winding current.

The MS31703NA can reduce electromagnetic interference (EMI) by the programmable slew rate control technology. It can also be applied flexibly and prevent any gate short-circuit issues.

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS31703NA	QFN32	MS31703NA

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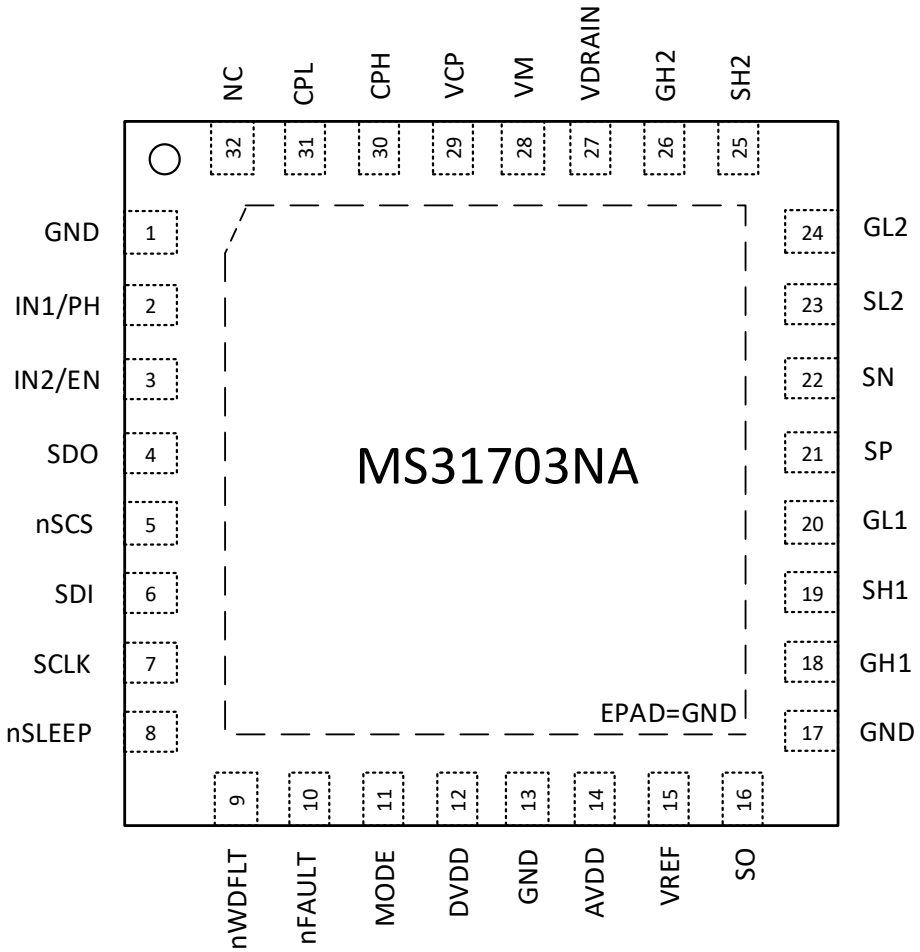
PIN CONFIGURATION

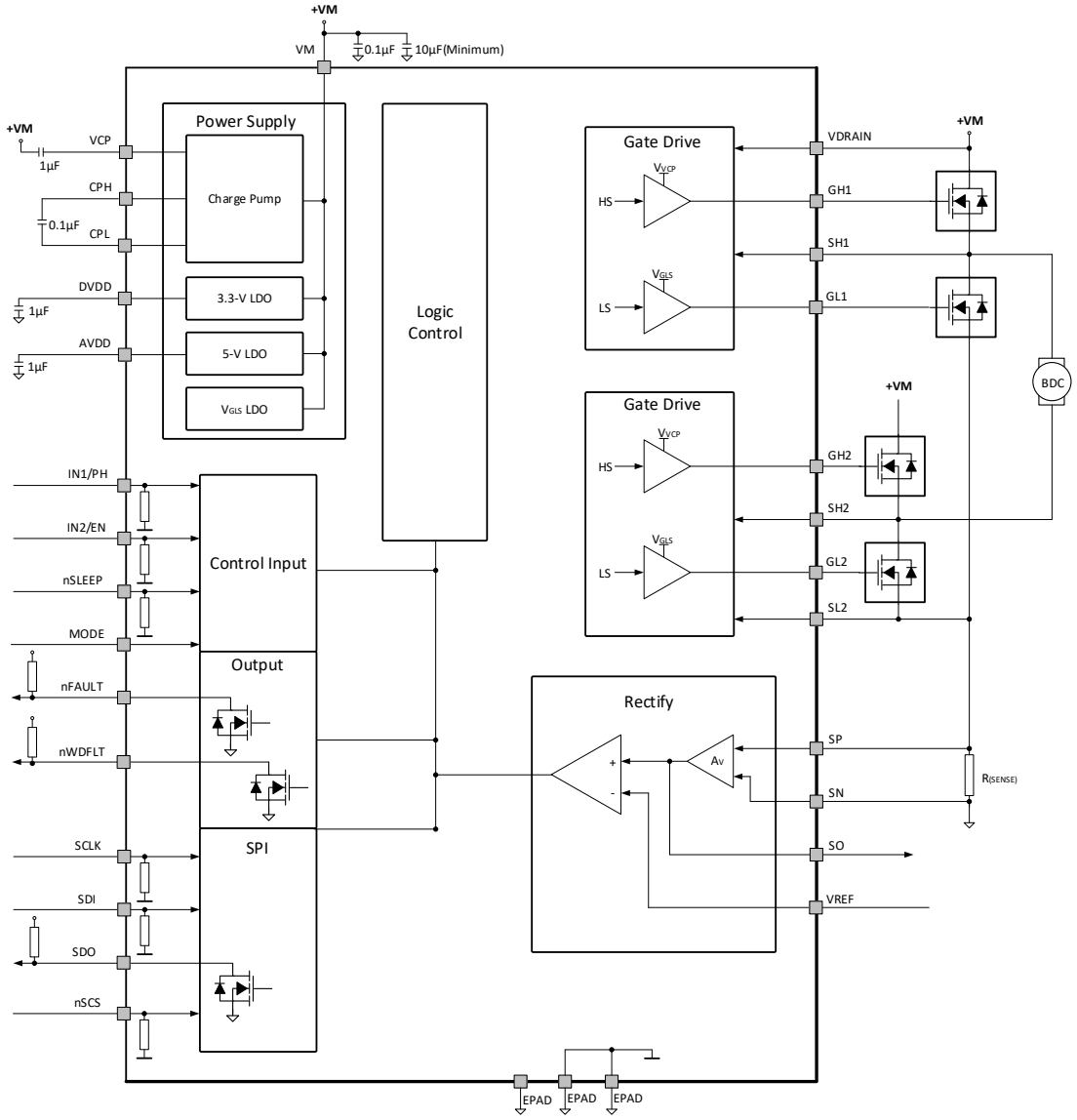


PIN DESCRIPTION

Pin	Name	Type	Description
GND	1	-	Ground.
IN1/PH	2	I	Input Control Pin. The logic of this pin depends on the MODE pin. This pin is connected to the ground with the internal pull-down resistor.
IN2/EN	3	I	Input Control Pin. The logic of this pin depends on the MODE pin. This pin is connected to the ground with the internal pull-down resistor.
SDO	4	O	SPI Data Output. This pin is open-drain output, which needs the external pull-up resistor.
nSCS	5	I	SPI Select Input. When this pin is pulled low, data input is enabled.
SDI	6	I	SPI Data Input. This pin is connected to the ground with the internal pull-down resistor.
SCLK	7	I	SPI Clock Input. This pin is connected to the ground with the internal pull-down resistor.
nSLEEP	8	I	Sleep Mode Input Pin. Pull this pin to logic low to make the device in low power dissipation sleep mode with the FET in high-impedance state (Hi-Z). This pin is connected to the ground with the internal pull-down resistor.
nWDFLT	9	O	Watchdog Fault Indication Pin. When the watchdog fault occurs, this pin is pulled low. This pin is open-drain output, which needs the external pull-up resistor.
nFAULT	10	O	Fault Indication Pin. When the fault occurs, this pin is pulled low. This pin is open-drain output, which needs the external pull-up resistor.
MODE	11	I	Mode Control Pin. When this pin is pulled to logic low, enabling EN/PH control mode. When this pin is pulled to logic high, enabling independent H-bridge mode. When this pin is hanging, enabling PWM control mode. When this pin is powered on or exits sleep mode, operation of this pin is latched. This pin is connected to the internal pull-up and pull-down resistors.

Pin	Name	Type	Description
DVDD	12	O	3.3V Logic Power Supply Output. This pin is connected to the ground with a 1μF bypass capacitor.
GND	13	-	Ground.
AVDD	14	O	5V Analog Power Supply Output. This pin is connected to the ground with a 1μF bypass capacitor.
VREF	15	I	Analog Reference Voltage Input. This pin controls chopping current.
SO	16	O	Shunt Amplifier Output. The capacitor on this pin can not exceed 1nF.
GND	17	-	Ground.
GH1	18	O	High-side Gate. Connect this pin to high-side FET gate.
SH1	19	I	High-side Source. Connect this pin to high-side FET source.
GL1	20	O	Low-side Gate. Connect this pin to low-side FET gate.
SP	21	I	Shunt Amplifier Positive Input. Connected to positive terminal of sense resistor.
SN	22	I	Shunt Amplifier Negative Input. Connected to negative terminal of sense resistor.
SL2	23	I	Low-side Source. Connect this pin to low-side FET source.
GL2	24	O	Low-side Gate. Connect this pin to low-side FET gate.
SH2	25	I	High-side Source. Connect this pin to high-side FET source.
GH2	26	O	High-side Gate. Connect this pin to high-side FET gate.
VDRAIN	27	I	High-side Drain. Connect this pin to high-side FET drain.
VM	28	-	Power Supply. Connect this pin to the motor power supply. This pin is connected to the ground with a 0.1μF and the minimum 10μF bypass capacitors.
VCP	29	I/O	Charge-pump Voltage. Connected to VM with a 1μF capacitor.
CPH	30	I/O	Charge-pump Capacitor Output.
CPL	31	I/O	Charge-pump Capacitor Input. Connected to CPH with a 0.1μF capacitor.
NC	32	-	Not Connection.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	VM	-0.3 ~ 47	V
Charge-pump Voltage	VCP, CPH	-0.3 ~ V_{VM}+12	V
Charge-pump Capacitor Input	CPL	-0.3 ~ V_{VM}	V
3.3V Logic Power Supply	DVDD	-0.3 ~ 3.8	V
5V Analog Power Supply	AVDD	-0.3 ~ 5.75	V
Drain Pin Voltage	VDRAIN	-0.3 ~ 47	V
Voltage Difference between VM and VDRAIN	VM - VDRAIN	-10 ~ 10	V
Logic Control Pin Voltage	IN1, IN2, nSLEEP, nFAULT, nWDFLT, VREF, MODE, nSCS, SCLK, SDI, SDO	-0.3 ~ 5.75	V
High-side Gate Pin Voltage	GH1, GH2	-0.3 ~ V_{VM}+12	V
Low-side Gate Pin Voltage	GL1, GL2	-0.3 ~ 12	V
High-side Source Pin Voltage	SH1, SH2	-1.2 ~ V_{VM}+1.2	V
Shunt Amplifier Input Pin Voltage	SP, SL2	-0.5 ~ 1.2	V
	SN	-0.3 ~ 0.3	V
Shunt Amplifier Output Pin Voltage	SO	-0.3 ~ 5.75	V
Shunt Amplifier Output Pin Current	SO	0 ~ 5	mA
VDRAIN Limit Current	I_{VDRAIN}	-2 ~ 2	mA
Open-drain Output Current	nFAULT, SDO, nWDFLT	0 ~ 10	mA
Gate Pin Source Current	GH1, GL1, GH2, GL2	0 ~ 250	mA
Gate Pin Sink Current	GH1, GL1, GH2, GL2	0 ~ 500	mA
Junction Temperature	T_J	-40 ~ 150	°C
Storage Temperature	T_{stg}	-65 ~ 150	°C
ESD(HBM)		±3000	V
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	°C/W

RECOMMENDED OPERATING CONGITIONS

Parameter	Symbol	Range			Unit
		Min	Typ	Max	
Power Supply	V_{VM}	5.5		45	V
Logic Voltage	V_{CC}	0		5.25	V
Shunt Amplifier Reference Voltage	V_{VREF}	0.3[1]		3.6	V
PWM Frequency	$f_{(PWM)}$			100	kHz
5V Analog Power Supply Current	I_{AVDD}			30[2]	mA
3.3V Logic Power Supply Current	I_{DVDD}			30[2]	mA
Shunt Amplifier Output Current	I_{SO}			5	mA
Operating Temperature	T_A	-40		125	°C

Note:

1. V_{VREF} must be operated from 0 to 0.3V, but the accuracy is relatively low.
2. Power dissipation and thermal limit must be observed.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A=25°C, V_{VM}=13.5V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply (VM, AVDD, DVDD)						
VM Power Supply	V_{VM}	Gate Drive Function	5.5		45	V
		Logic Function	4.5		45	
VM Power Supply Current	I_{VM}	V_{VM}=13.5V, nSLEEP=1		6.0		mA
VM Sleep Mode Current	$I_{(SLEEP)}$	nSLEEP=0,V_{VM}=13.5V, T_A=25°C		13		µA
		nSLEEP=0,V_{VM}=13.5V, T_A=125°C			30	
DVDD Output Voltage	V_{DVDD}	2mA Load		3.3		V
		30mA Load, V_{VM}=13.5V		3.2		
AVDD Output Voltage	V_{AVDD}	2mA Load		5.0		V
		30mA Load, V_{VM}=13.5V		5.0		
Charge-pump (VCP, CPH, CPL)						
VCP Power Supply	V_{VCP}	V_{VM}=13.5V		23.8		V
		V_{VM}=8V		14.7		
		V_{VM}=5.5V		9.7		
Charge-pump Current Capacity	I_{VCP}	V_{VM}>13.5V	9.5			mA
		8V<V_{VM}<13.5V	9.5			
		5.5V<V_{VM}<8V	7.5			
Control Inputs(IN1/PH, IN2/EN, nSLEEP, MODE, nSCS, SCLK, SDI)						
Logic Low Input Voltage	V_{IL}		0		0.8	V
Logic High Input Voltage	V_{IH}		1.5		5.25	V
Logic Input Hysteresis	V_{hys}		100			mV
Logic Low Input Current	I_{IL}	V_{IN}=0V, IN1/PH, IN2/EN, nSLEEP, nSCS, SCLK, SDI	-5		5	µA
		V_{IN}=0V, MODE			80	µA
Logic High Input Current	I_{IH}	V_{IN}=5V, IN1/PH, IN2/EN, nSLEEP, nSCS, SCLK, SDI			70	µA
		V_{IN}=5V, MODE			120	µA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Pull-down Resistance	R_{PD}	IN1/PH, IN2/EN, nSLEEP, nSCS, SCLK, SDI		100		kΩ
		MODE		55		kΩ
Pull-up Resistance	R_{PU}	MODE		26		kΩ
Control Outputs(nFAULT, nWDFLT, SDO)						
Logic Low Output Voltage	V_{OL}	I_O=2mA			0.1	V
High-impedance Output Drain Current	I_{OZ}	5V Pull-up Voltage	-2		2	μA
FET Gate Driver(GH1, GH2, SH1, SH2, GL1, GL2)						
High-side V_{GS} Gate Driver(Gate to Source)	V_{GSH}	V_{VM}>13.5V, Using SHx as a Reference		10.5	11.5	V
		V_{VM}=8V, Using SHx as a Reference	5.7		6.8	
		V_{VM}=5.5V, Using SHx as a Reference	3.4		4.3	
Low-side V_{GS} Gate Driver	V_{GSL}	V_{VM}>10.5V		10.5		
		V_{VM}<10.5V	V_{VM}-2			
High-side Source Current Peak(V_{VM}=13.5V)	I_{DRIVE} (SRC_HS)	IDRIVE=3'b000		14		mA
		IDRIVE=3'b001		28		
		IDRIVE=3'b010		65		
		IDRIVE=3'b011		92		
		IDRIVE=3'b100		130		
		IDRIVE=3'b101		183		
		IDRIVE=3'b110		221		
		IDRIVE=3'b111		248		

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-side Sink Current Peak(V_{VM}=13.5V)	I_{DRIVE} (SNK_HS)	IDRIVE=3'b000		21		mA
		IDRIVE=3'b001		41		
		IDRIVE=3'b010		99		
		IDRIVE=3'b011		136		
		IDRIVE=3'b100		190		
		IDRIVE=3'b101		252		
		IDRIVE=3'b110		322		
		IDRIVE=3'b111		383		
Low-side Source Current Peak(V_{VM}=13.5V)	I_{DRIVE} (SRC_LS)	IDRIVE=3'b000		10		mA
		IDRIVE=3'b001		20		
		IDRIVE=3'b010		49		
		IDRIVE=3'b011		68		
		IDRIVE=3'b100		99		
		IDRIVE=3'b101		132		
		IDRIVE=3'b110		179		
		IDRIVE=3'b111		230		
Low-side Sink Current Peak(V_{VM}=13.5V)	I_{DRIVE} (SNK_LS)	IDRIVE=3'b000		21		mA
		IDRIVE=3'b001		42		
		IDRIVE=3'b010		96		
		IDRIVE=3'b011		136		
		IDRIVE=3'b100		196		
		IDRIVE=3'b101		250		
		IDRIVE=3'b110		334		
		IDRIVE=3'b111		423		
FET Holding Current	I_{HOLD}	Pull-up Current after t_{DRIVE}, GHx		10		mA
		Pull-up Current after t_{DRIVE}, GLx		40		

Parameter	Symbol	Condition	Min	Typ	Max	Unit
FET Strong Pull-down Current	I_{STRONG}	GHx		750		mA
		GLx		1000		
FET Gate Holding Resistor	$R_{(OFF)}$	Pull-down GHx to SHx		150		kΩ
		Pull-down GLx to GND		150		
Shunt Amplifier and PWM Current Control (SP, SN, SO, VREF)						
VREF Input RMS Voltage	V_{VREF}	Used for Internal Chopping Current Control	0.3		3.6	V
VREF Input Impedance	R_{VREF}	VREF_SCL=00 (100%)	1			MΩ
		VREF_SCL=01,10,11		175		kΩ
Amplifier Gain	A_V	GAIN_CS=00, 10<V_{SP}<450mV, V_{SN}=GND		10		V/V
		GAIN_CS=01, 60<V_{SP}<225mV, V_{SN}=GND		20		
		GAIN_CS=10, 10<V_{SP}<112mV, V_{SN}=GND		40		
		GAIN_CS=11, 10<V_{SP}<56mV, V_{SN}=GND		80		
Input Offset Voltage	V_{IO}	V_{SP}=V_{SN}=GND		5	10	mV
Input Offset Voltage Temperature Drift	$V_{IO(DRIFT)}$	V_{SP}=V_{SN}=GND		10		μV/°C
SP Input Current	I_{SP}	V_{SP}=100mV, V_{SN}=GND		-50		μA
SO Output Voltage Range	V_{SO}		Av×V_{IO}		4.5	V
SO Pin Capacitance	$C_{(SO)}$				1	nF

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Protection Circuit						
VM Undervoltage Protection	$V_{(UVLO2)}$	VM Falling, UVLO2 Alarm Threshold		5.25		V
		VM Rising, UVLO2 Recovery Threshold		5.4		
VM Logic Undervoltage Lockout	$V_{(UVLO1)}$				4.5	V
VM Undervoltage Hysteresis	$V_{hys\ (UVLO)}$	Rising to falling	100			mV
Charge-pump Undervoltage Protection	$V_{(CP\_UV)}$	VCP Falling, CPUV Alarm Threshold		VM+1.5		V
		VCP Rising, CPUV Recovery Threshold		VM+1.55		
Charge-pump Undervoltage Hysteresis	$V_{hys\ (CP\_UV)}$	Rising to Falling		50		mV
V_{DS} Overcurrent Protection Threshold (V_{DS} of External FET)	$V_{DS(OCP)}$	VDS=3'b000		0.06		V
		VDS=3'b001		0.14		
		VDS=3'b010		0.17		
		VDS=3'b011		0.2		
		VDS=3'b100		0.12		
		VDS=3'b101		0.24		
		VDS=3'b110		0.48		
		VDS=3'b111		0.96		
V_{SP} Overcurrent Protection Threshold, Measured by the Amplifier	$V_{SP(OCP)}$	V_{SP} Relative to GND		1		V
Over-temperature Warning Temperature	$T_{(OTW)}$		120	135	145	°C
Over-temperature Protection Temperature	T_{SD}		150			°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Over-temperature Protection Hysteresis	T_{hys}			20		℃
Gate Drive Clamp Voltage	$V_{C(GS)}$	Positive Clamp Voltage		14		V
		Negative Clamp Voltage		-0.7		
Switching Characteristics						
Power Supply(VM, AVDD, DVDD)						
Sleep Time	$t_{(SLEEP)}$	nSLEEP=0 to Sleep Start			110	μs
Wake-up Time	$t_{(wu)}$	nSLEEP=1 to Output Changes			1.1	ms
Turn-on Time	t_{on}	VM>UVLO2 to Output Changes			1.1	ms
Charge-pump (VCP, CPH, CPL)						
Charge-pump Switching Frequency	$f_{S(VCP)}$	VM>UVLO2	200	400	700	kHz
Control Inputs (IN1, IN2, nSLEEP, MODE, nSCS, SCLK, SDI, PH, EN)						
Propagation Delay	t_{pd}	IN1, IN2 to GHx or GLx		500		ns
FET Gate Driver (GH1, GH2, SH1, SH2, GL1, GL2)						
Dead Time	$t_{(DEAD)}$	TDEAD=2'b00		130		ns
		TDEAD=2'b01		260		
		TDEAD=2'b10		520		
		TDEAD=2'b11		1040		
Gate Drive Time	$t_{(DRIVE)}$			2.75		μs
Shunt Amplifier and PWM Current Control (SP, SN, SO, VREF)						
Setup Time	t_S	V_{SP}=V_{SN}=GND to V_{SP}=240mV, V_{SN}=GND, A_V=10, $C_{(SO)}$=200pF			0.5	μs
		V_{SP}=V_{SN}=GND to V_{SP}=120mV, V_{SN}=GND, A_V=20, $C_{(SO)}$=200pF			1	
		V_{SP}=V_{SN}=GND to V_{SP}=60mV, V_{SN}=GND, A_V=40, $C_{(SO)}$=200pF			2	

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Setup Time	t_S	V_{SP}=V_{SN}=GND to V_{SP}=30mV, V_{SN}=GND, A_V=80, $C_{(SO)}$=200pF			4	μs
PWM Off-time	t_{off}	TOFF=00		27.5		μs
		TOFF=01		55		
		TOFF=10		110		
		TOFF=11		220		
PWM Blanking Time	$t_{(BLANK)}$			2.2		μs
VM Undervoltage Detect Time	$t_{(UVLO)}$	VM Falling, UVLO Alarm		11		μs
Overcurrent Detect Time	$t_{(OCP)}$			4.4		μs
Overcurrent Off-time	$t_{(RETRY)}$			3.3		ms
Watchdog Timeout Threshold	$t_{(WD)}$	WD_DLY=2'b00		11		ms
		WD_DLY=2'b01		22		
		WD_DLY=2'b10		55		
		WD_DLY=2'b11		110		
Watchdog Timer Reset Cycle	$t_{(RESET)}$			70		μs

FUNCTION DESCRIPTION

The MS31703NA controls four external NMOSFETs to drive bidirectional brushed DC motors. The MS31703NA can also operate in independent H-bridge mode to drive two directional brushed DC motors. It supports power supply from 5.5V to 45V and enables low power dissipation sleep mode through the nSLEEP pin. The control mode has three options, including configurable PH/EN, independent H-bridge control or PWM mode, which is easy to be connected with controller circuit.

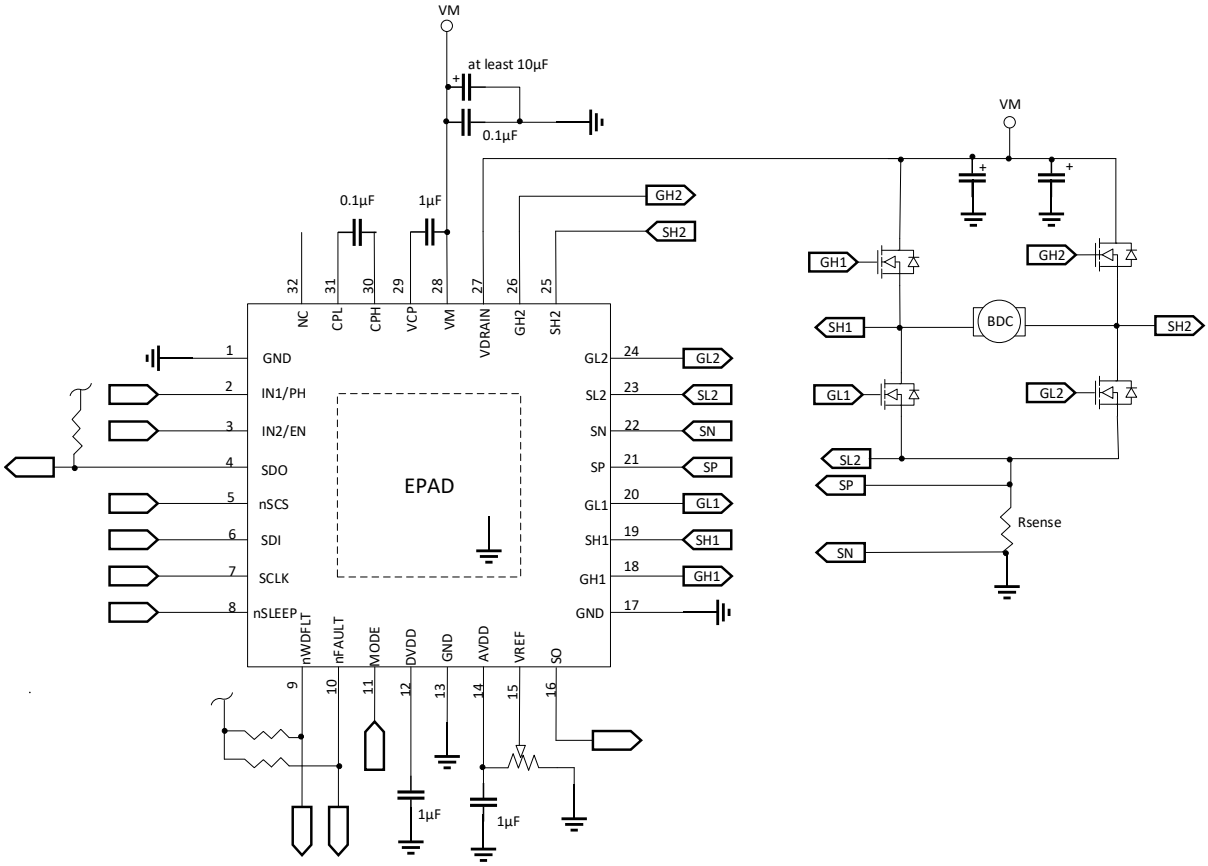
The MS31703NA can adjust gate drive strength or gate drive current to optimize different FET applications without external resistors. The device number of motor drive systems are strikingly reduced by integrating the needed FET drive circuits into the single device. The peak current can be adjusted through SPI. When VM voltage is more than 13.5V, high-side and low-side FETs are driven with 10.5V (nominal) gate source voltage (VGS). At lower VM voltage, the VGS is reduced. The high-side gate drive voltage is generated through a double-structure charge-pump that regulated to VM+10.5V.

The shunt amplifier gain of the MS31703NA can be configured through SPI. The current can be limited by the current chopping way with internal fixed off-time.

The MS31703NA has complete protection functions, including: undervoltage lockout(UVLO), overcurrent protection(OCP), gate drive faults and thermal shutdown(TSD).

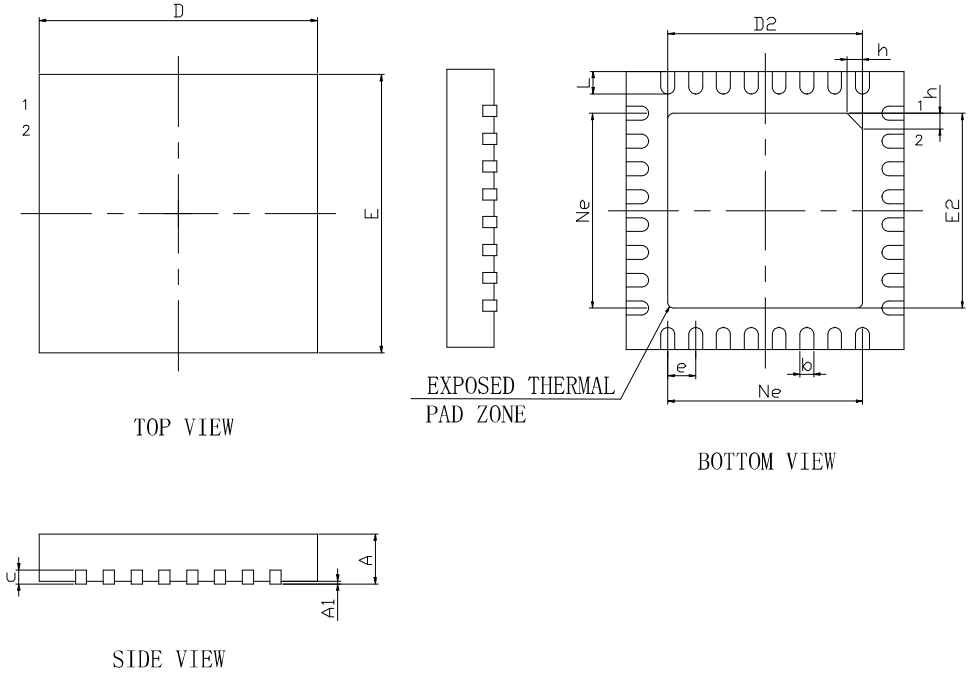
The MS31703NA integrates the spread spectrum clock function of internal digital oscillator and charge pumps, which is combined with output conversion rate to minimize radiation.

TYPICAL APPLICATION



PACKAGE OUTLINE DIMENSIONS

QFN32



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description

Product Name: MS31703NA

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS31703NA	QFN32	1000	8	8000	4	32000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.