

2kSPS, 24bit Σ - Δ ADC

FEATURES

- Programmable Conversion Rate: 2kSPS (Max)
- Integrated Input Multiplexer
- PGA Noise: 70nV (RMS)@PGA=128
- Dual-Matched Programmable Current Source
- Integrated Low Temperature Drift 2.048V Voltage Reference
- Integrate Internal Temperature Sensor
- Integrate Power Detection Circuit and VREF Detection Circuit
- Integrated Self-calibration and System Calibration
- Compatible with SPI Interface
- Integrated 50Hz/60Hz Rejection Filter (Conversion Rate 20SPS)
- Analog Power Supply:
Unipolar Power Supply: 2.7V to 5.25V
Bipolar Power Supply: $\pm 2.5V$
- Operating Temperature Range: $-40^{\circ}C$ to $125^{\circ}C$

APPLICATIONS

- Stress Detection
- Temperature Detection
- Gas Analysis and Blood Analysis
- Industrial Process Control and Instrumentation

PRODUCT DESCRIPTION

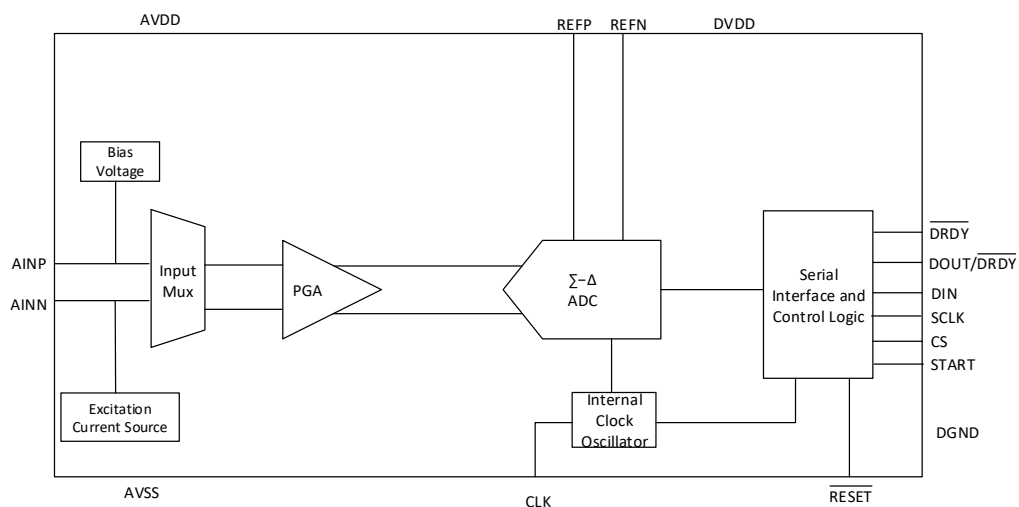
The MS5146T/MS5147T/MS5148T is a 24bit ADC and is suitable for high-precision and low-cost measurement application. It integrates low-noise programmable gain amplifier, high-precision ADC and internal oscillator. The MS5147T and MS5148T integrate low temperature drift reference and dual-matched programmable current source. The MS5148T supports four differential inputs. The MS5147T supports two differential inputs. The MS5146T supports single differential input. In addition, the MS514XT series also integrate sensor detection Burnout current source and bias voltage generator.

The MS5146T is available in TSSOP16 package. The MS5147T is available in TSSOP20 package. The MS5148T is available in TSSOP28 package.

PRODUCT SPECIFICATION

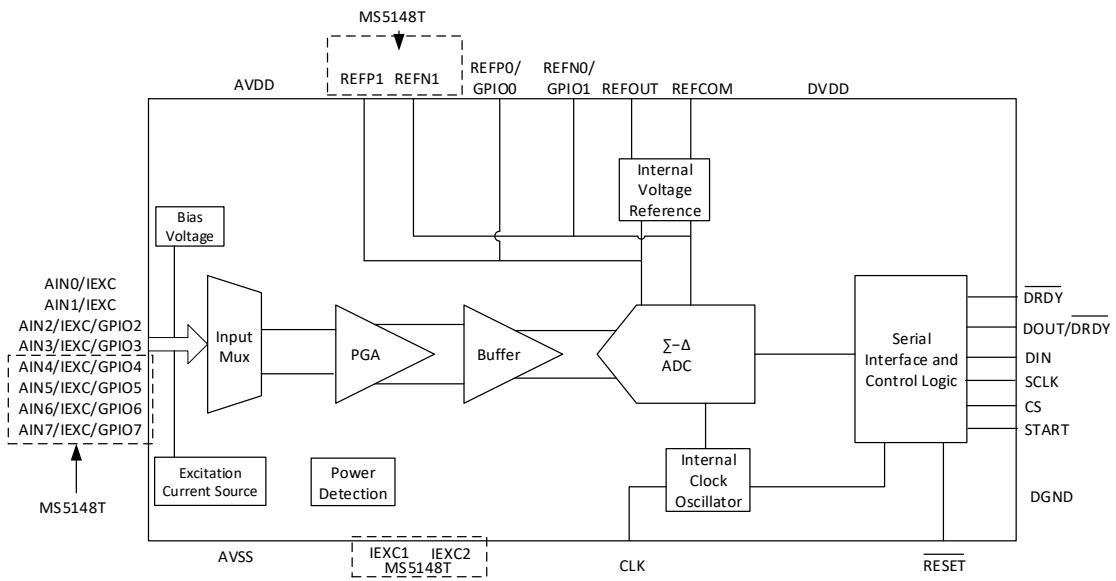
Part Number	Package	Marking
MS5146T	TSSOP16	MS5146T
MS5147T	TSSOP20	MS5147T
MS5148T	TSSOP28	MS5148T

BLOCK DIAGRAM



MS5146T Block Diagram





MS5147T, MS5148T Block Diagram

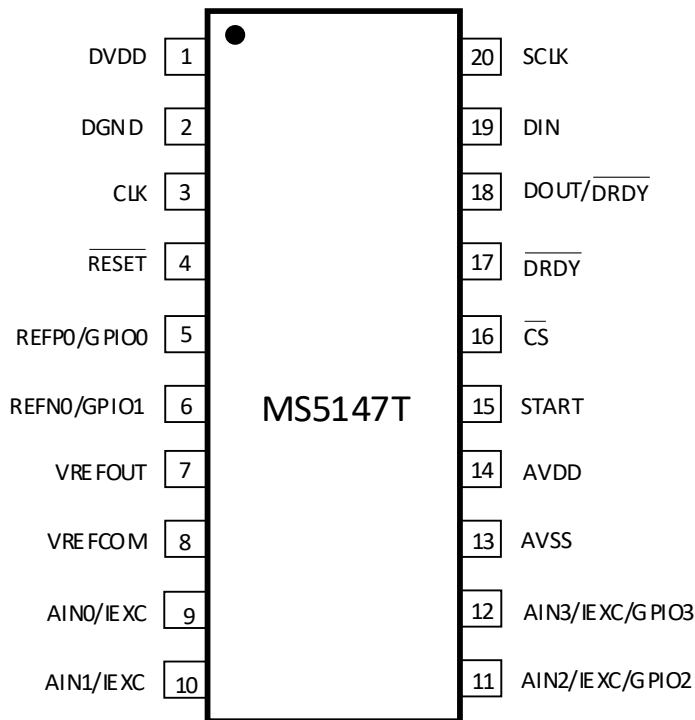
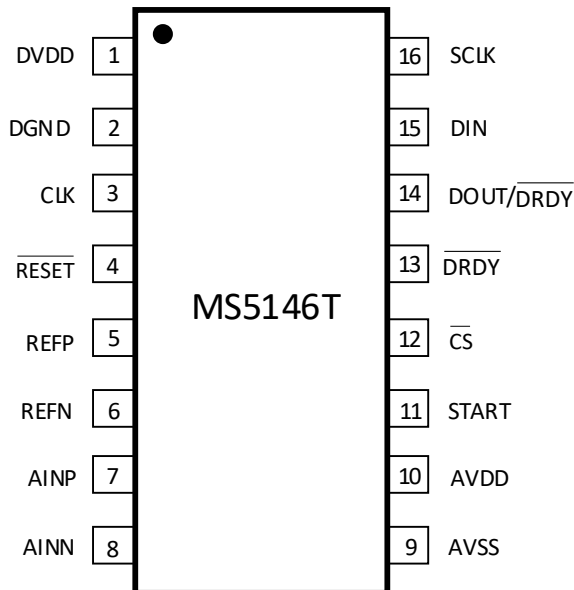


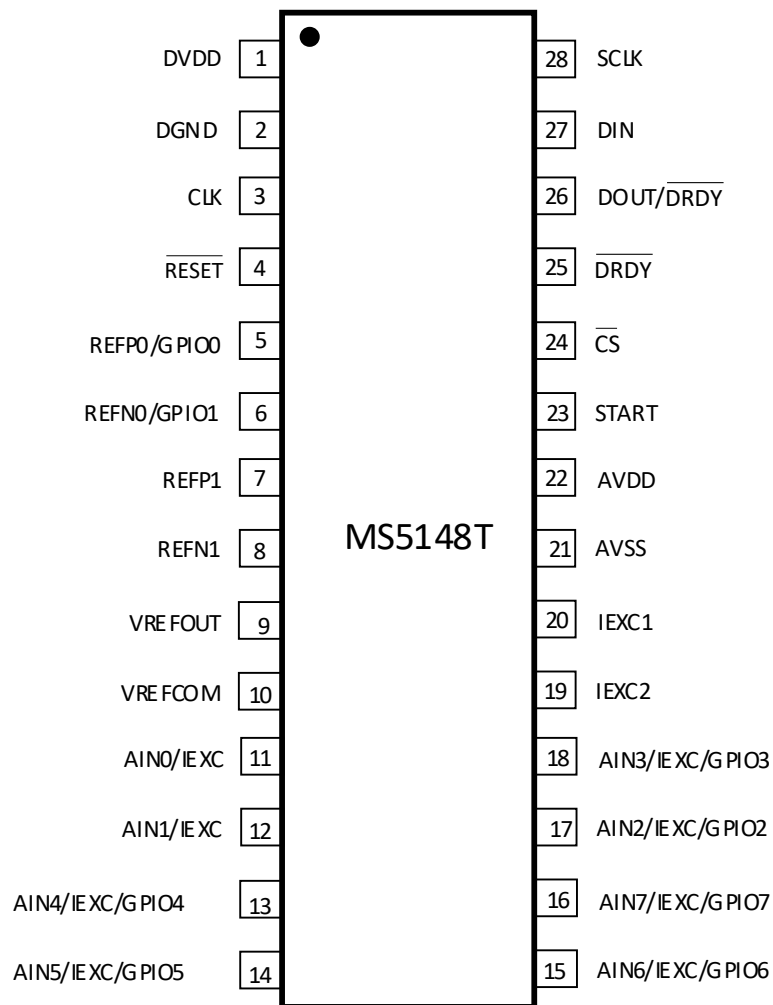
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PIN CONFIGURATION





PIN DESCRIPTION

Pin	Name	Type	Description
MS5146T			
1	DVDD	-	Digital Power Supply
2	DGND	-	Digital Ground
3	CLK	I	External Clock input. Internal is activated when the pin is grounded.
4	$\overline{\text{RESET}}$	I	Reset, Active Low.
5	REFP	I	External Reference, Positive Terminal
6	REFN	I	External Reference, Negative Terminal
7	AINP	I	Analog Input, Positive Terminal
8	AINN	I	Analog Input, Negative Terminal
9	AVSS	-	Negative Power Supply
10	AVDD	-	Positive Power Supply
11	START	I	Conversion Start Signal
12	$\overline{\text{CS}}$	I	Chip Select, Active Low.
13	$\overline{\text{DRDY}}$	O	Data Ready, Active Low.
14	DOUT/ $\overline{\text{DRDY}}$	O	Serial Data Output or Data Output with Data Ready
15	DIN	I	Serial Data Input
16	SCLK	I	Serial Clock Input
MS5147T			
1	DVDD	-	Digital Power Supply
2	DGND	-	Digital Ground
3	CLK	I	External Clock input. Internal is activated when the pin is grounded.
4	$\overline{\text{RESET}}$	I	Reset, Active Low.
5	REFP0/GPIO0	I/O	External Positive Reference Input 0 or Configured as Digital Input/Output 0.
6	REFN0/GPIO1	I/O	External Negative Reference Input 0 or Configured as Digital Input/Output 1.
7	VREFOUT	O	Internal Reference Positive Output.
8	VREFCOM	O	Internal Reference Negative Output. VREFCOM is connected to AVSS when using single power supply. VREFCOM is connected to mid-voltage of two power supplies when using bipolar power supply.
9	AIN0/IEXC	I/O	Analog Input 0 or Optional Excitation Current Output
10	AIN1/IEXC	I/O	Analog Input 1 or Optional Excitation Current Output



Pin	Name	Type	Description
11	AIN2/IEXC/ GPIO2	I/O	Analog Input 2 or Optional Excitation Current Output or Configured as Digital Input/Output 2.
12	AIN3/IEXC/ GPIO3	I/O	Analog Input 3 or Optional Excitation Current Output or Configured as Digital Input/Output 3.
13	AVSS	-	Negative Power Supply
14	AVDD	-	Positive Power Supply
15	START	I	Conversion Start Signal
16	\overline{CS}	I	Chip Select, Active Low.
17	\overline{DRDY}	O	Data Ready, Active Low.
18	DOUT/ \overline{DRDY}	O	Serial Data Output or Data Output with Data Ready
19	DIN	I	Serial Data Input
20	SCLK	I	Serial Clock Input
MS5148T			
1	DVDD	-	Digital Power Supply
2	DGND	-	Digital Ground
3	CLK	I	External Clock input. Internal is activated when the pin is grounded.
4	\overline{RESET}	I	Reset, Active Low.
5	REFP0/GPIO0	I/O	External Positive Reference Input 0 or Configured as Digital Input/Output 0.
6	REFN0/GPIO1	I/O	External Negative Reference Input 0 or Configured as Digital Input/Output 1.
7	REFP1	I	External Positive Reference Input 1.
8	REFN1	I	External Negative Reference Input 1.
9	VREFOUT	O	Internal Reference Positive Output.
10	VREFCOM	O	Internal Reference Negative Output. VREFCOM is connected to AVSS when using single power supply. VREFCOM is connected to mid-voltage of two power supplies when using bipolar power supply.
11	AIN0/IEXC	I/O	Analog Input 0 or Optional Excitation Current Output
12	AIN1/IEXC	I/O	Analog Input 1 or Optional Excitation Current Output
13	AIN4/IEXC/ GPIO4	I/O	Analog Input 4 or Optional Excitation Current Output or Configured as Digital Input/Output 4.
14	AIN5/IEXC/ GPIO5	I/O	Analog Input 5 or Optional Excitation Current Output or Configured as Digital Input/Output 5.



Pin	Name	Type	Description
15	AIN6/IEXC/ GPIO6	I/O	Analog Input 6 or Optional Excitation Current Output or Configured as Digital Input/Output 6.
16	AIN7/IEXC/ GPIO7	I/O	Analog Input 7 or Optional Excitation Current Output or Configured as Digital Input/Output 7.
17	AIN2/IEXC/ GPIO2	I/O	Analog Input 2 or Optional Excitation Current Output or Configured as Digital Input/Output 2.
18	AIN3/IEXC/ GPIO3	I/O	Analog Input 3 or Optional Excitation Current Output or Configured as Digital Input/Output 3.
19	IEXC2	O	Excitation Current Output 2
20	IEXC1	O	Excitation Current Output 1
21	AVSS	-	Negative Power Supply
22	AVDD	-	Positive Power Supply
23	START	I	Conversion Start Signal
24	$\overline{\text{CS}}$	I	Chip Select, Active Low.
25	$\overline{\text{DRDY}}$	O	Data Ready, Active Low.
26	DOUT/ $\overline{\text{DRDY}}$	O	Serial Data Output or Data Output with Data Ready
27	DIN	I	Serial Data Input
28	SCLK	I	Serial Clock Input



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Analog Power Supply	AVDD to AVSS	-0.3 ~ +7.0	V
Digital Power Supply	VDVDD	-0.3 ~ +7.0	V
Analog Input Voltage	VAINX, VIEXC1, VIEXC2	VAVSS-0.3 ~ VAVDD+0.3	V
Reference Voltage	VREFPX, VREFNX, VREFOUT, VREFCOM	-0.3 ~ VAVDD+0.3	V
Digital Input Voltage		-0.3 ~ VDVDD+0.3	V
Digital Output Voltage	V _(LE)	-0.3 ~ VDVDD+0.3	V
Input Port Current		10	mA
Storage Temperature	T _{STG}	-65 ~ 150	°C
Lead Temperature(10s)		260	°C
ESD(HBM)	V _{ESD}	±2000	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Analog Power Supply	AVDD to AVSS	2.7		5.25	V
	AVSS to DGND	-2.65		0.1	
	AVDD to DGND	2.25		5.25	
Digital Power Supply	DVDD to DGND	2.7		5.25	V
Analog Differential Input	V _(AINP-AINN)	-V _{REF} /GAIN		+V _{REF} /GAIN	V
Reference Voltage Differential Input	V _{REFP} - V _{REFN}	0.5		(V _{AVDD} -V _{AVSS})-1	V
Reference Voltage Positive Input		V _{REFN} + 0.5		V _{AVDD} + 0.1	V
Reference Voltage Negative Input		V _{AVSS} - 0.1		V _{REFP} - 0.5	V
External Clock Input		1		4.5	MHz
External Clock Input Duty		25		75	%
GPIO Input Voltage		V _{AVSS}		V _{AVDD}	V
Digital Input Voltage		V _{DVSS}		V _{DVDD}	V
Operating Temperature	T _A	-40		125	°C



ELECTRICAL CHARACTERISTICS
 $V_{AVDD}=5V$, $V_{DVDD}=3.3V$, $V_{AVSS}=0V$, External $V_{REF}=2.048V$, $f_{CLK}=4.096MHz$.

Unless otherwise noted, all parameters are in full temperature range.

Parameter	Condition	Min	Typ	Max	Unit
Analog Input					
Different Input Current			100		pA
Input impedance	DR=5SPS, 10SPS, 20SPS		5000		MΩ
	DR=40SPS, 80SPS, 160SPS		1200		
	DR=320SPS, 640SPS, 1kSPS		600		
	DR=2kSPS		300		
System Performance					
Resolution			24		Bits
Conversion Rate		5		2k	SPS
Integral Non-linearity (INL)	Differential Input, GAIN=1, $V_{CM}=2.5V$		10		ppm
Zero-scale Offset (V_{io})	After Calibration	-15		15	μV
Gain Error	DR=40SPS, 80SPS, 160SPS	-0.02	± 0.01	0.02	%
Common-mode Rejection	GAIN=1		90		dB
	GAIN=32		125		
Power Supply Rejection	GAIN=32, DR=80SPS		100		dB
Reference Voltage Input					
Reference Input Current			30		nA
Internal Reference Voltage					
Internal Reference Output Voltage		2.038	2.048	2.058	V
Internal Reference Temperature Drift	$T_A=-40^{\circ}C$ to $125^{\circ}C$		10		ppm/ $^{\circ}C$
Output Current			10		mA
Load Regulation			50		$\mu V/mA$
Setup Time		See "Internal Reference Voltage"			
Internal Oscillator					
Internal Clock Frequency		3.9	4.096	4.25	MHz
Excitation Current Source					
Output Current		50,100,250,500,750,1000,1500			μA
Output Current Error		-6	± 1	+6	%



Parameter	Condition	Min	Typ	Max	Unit
Output Current Match			±0.15		%
Output Current Temperature Drift			100		ppm/°C
Output Current Match Temperature Drift			10		ppm/°C
Bias Voltage					
Bias Voltage		0.5×(V _{AVDD} +V _{AVSS})			V
Bias Voltage Output Impedance			400		Ω
Temperature Sensor					
Output Voltage	T _A =25°C		110		mV
Output Voltage Temperature Drift			375		μV/°C
General Input/Output Port (GPIO)					
Low-level Input Voltage (V _{IL})		V _{AVSS}		0.3×V _{AVDD}	V
High-level Input Voltage (V _{IH})		0.7×V _{AVDD}		V _{AVDD}	V
Low-level Output Voltage (V _{OL})	I _{OL} =1mA			0.2×V _{AVDD}	V
High-level Output Voltage (V _{OH})	I _{OH} =1mA	0.8×V _{AVDD}			V
Digital Input/Output Port (Not GPIO)					
Low-level Input Voltage (V _{IL})		DGND		0.3×V _{DVDD}	V
High-level Input Voltage (V _{IH})		0.7×V _{DVDD}		V _{DVDD}	V
Low-level Output Voltage (V _{OL})	I _{OL} =1mA	DGND		0.2×V _{DVDD}	V
High-level Output Voltage (V _{OH})	I _{OH} =1mA	0.8×V _{DVDD}			V
Input Leakage Current	DGND<V _{IN} <V _{DVDD}		±10		μA
Power Performance					
Analog Power Supply Current (I _{AVDD})	Power-down Mode		0.1		μA
	V _{AVDD} =3.3V, DR=20SPS, External Reference		221		
	Extra current after using internal reference		180		
Digital Power Supply Current (I _{DVDD})	Power-down Mode		0.2		μA
	V _{AVDD} =3.3V, DR=20SPS, External Reference		210		
Power Dissipation (P _D)	V _{AVDD} =V _{DVDD} =3.3V, DR=20SPS, Internal Oscillator, External Reference		1.4		mW



TIMING CHARACTERISTICS

$V_{DVDD}=2.7V$ to $5.25V$, $DGND=0V$, Input Logic 1=DVDD, Input Logic 0=GND.

Unless otherwise noted, all parameters are in full temperature range.

Parameter	Symbol	Min	Typ	Max	Unit
Delay Time, \overline{CS} Falling Edge to SCLK First Rising Edge	t_{CSSC}	10			ns
Delay Time, SCLK Last Falling Edge to \overline{CS} Rising Edge	t_{SCCS}	7			t_{CLK}^1
Pulse Width (\overline{CS} High-level)	t_{CSPW}	5			t_{CLK}
SCLK Period	t_{SCLK}	488			ns
Pulse Width (SCLK High-level)	t_{SPWH}	0.25		0.75	t_{SCLK}
Pulse Width (SCLK Low-level)	t_{SPWL}	0.25		0.75	t_{SCLK}
Setup Time (DIN Valid to SCLK Falling Edge)	t_{DIST}	5			ns
Hold Time (SCLK Falling Edge to DIN Valid)	t_{DIHD}	5			ns
Setup Time (SCLK Low-level to \overline{DRDY} Falling Edge)	t_{STD}	5			t_{CLK}
Hold Time (\overline{DRDY} Falling Edge to SCLK Rising Edge)	t_{DTS}	1			t_{CLK}
Pulse Width (START High-level)	t_{START}	3			t_{CLK}
Pulse Width (\overline{RESET} Low-level)	$t_{\overline{RESET}}$	4			t_{CLK}
Delay Time, \overline{RESET} Rising Edge to SCLK Rising Edge	t_{RHSC}	2^2			ms

Note:

- $t_{CLK} = 1 / f_{CLK}$. Default clock frequency $f_{CLK} = 4.096$ MHz.
- Decided by f_{CLK} . The value is valid when $f_{CLK} = 4.096$ MHz.

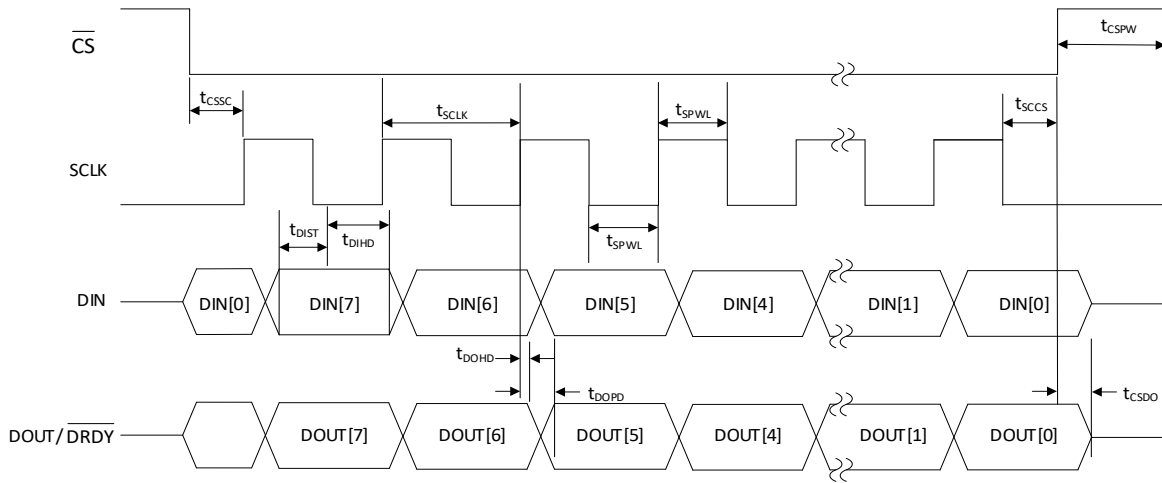
SWITCH CHARACTERISTICS

$V_{DVDD}=2.7V$ to $5.25V$, $DGND=0V$, Input Logic1=DVDD, Input Logic 0=GND.

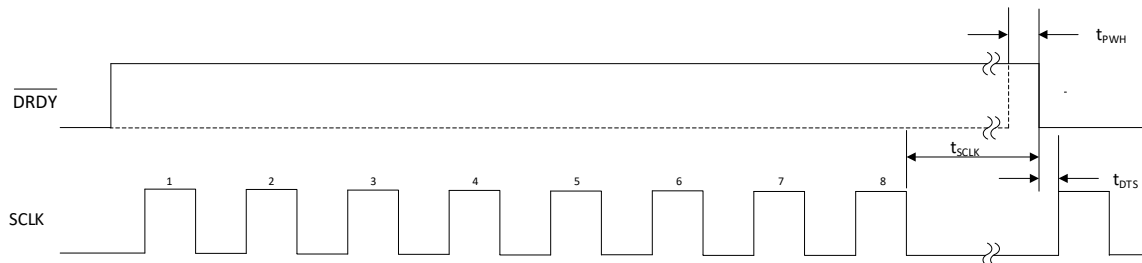
Unless otherwise noted, all parameters are in full temperature range.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Propagation Delay Time, SCLK Rising Edge to DOUT Valid	t_{DOPD}	$V_{DVDD} \leq 3.6V$			50	ns
		$V_{DVDD} > 3.6V$			180	
DOUT Hold Time	t_{DOHD}		0			ns
Propagation Delay Time, \overline{CS} Rising Edge to DOUT High-impedance	t_{CSPD}				10	ns
\overline{DRDY} High-level Pulse Width	t_{PWH}		3			t_{CLK}

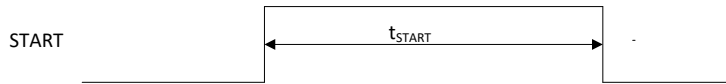




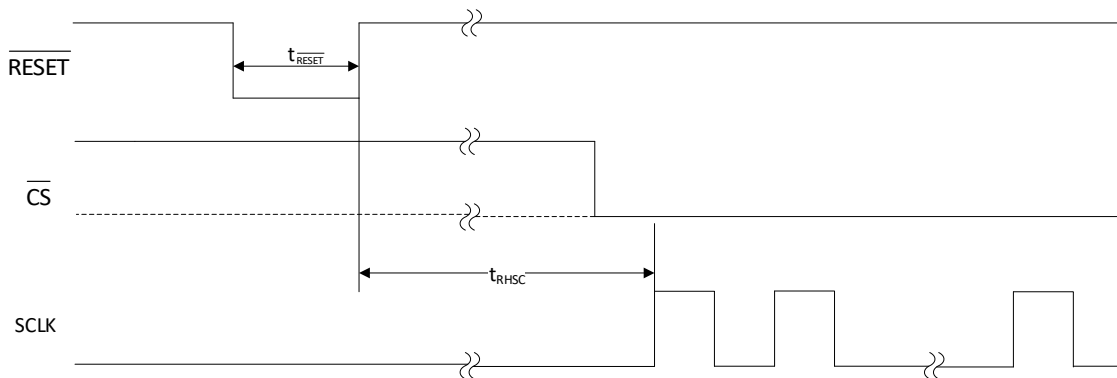
Read/Write Interface Timing, DRDY MODE Bit = 0



Data Ready Interface Timing



START Minimum Pulse Width



RESET Pulse Width and Interface Communication Timing after Reset



OUTPUT NOISE and RESOLUTION (EXTERNAL REFERENCE)

The table below gives the output RMS noise for the MS5148T with some gain and conversion rate settings. These data are for bipolar input range and 2.5V external reference voltage. These values are typical when the differential input voltage is 0V. It is important to note that the effective resolution is calculated from root mean square noise. These values are typical values and rounded to nearest LSB.

 Table 1. Output RMS Noise (μV) VS. Gain and Conversion Rate ($V_{\text{AVDD}}=5.0\text{V}$, $V_{\text{AVSS}}=0\text{V}$, External 2.5V Reference Voltage)

Conversion Rate	Gain 1	Gain 2	Gain 4	Gain 8	Gain 16	Gain 32	Gain 64	Gain 128
5	2.286	1.170	0.568	0.312	0.159	0.085	0.079	0.073
10	2.808	1.434	0.662	0.386	0.196	0.106	0.104	0.099
20	3.633	1.864	0.896	0.482	0.251	0.139	0.133	0.132
40	6.151	3.023	1.532	0.789	0.392	0.215	0.204	0.134
80	8.210	4.085	2.013	1.038	0.539	0.300	0.277	0.188
160	11.248	5.880	2.745	1.458	0.738	0.416	0.389	0.260
320	21.851	11.834	5.917	2.933	1.519	0.791	0.481	0.358
640	28.616	16.101	8.344	4.186	2.188	1.143	0.686	0.513
1000	34.540	21.334	10.847	5.531	2.783	1.487	0.883	0.645
2000	47.735	23.419	12.045	5.908	3.053	1.711	1.102	0.884

 Table 2. Effective Resolution VS. Gain and Conversion Rate ($V_{\text{AVDD}}=5.0\text{V}$, $V_{\text{AVSS}}=0\text{V}$, External 2.5V Reference Voltage)

Conversion Rate	Gain 1	Gain 2	Gain 4	Gain 8	Gain 16	Gain 32	Gain 64	Gain 128
5	20.8	20.7	20.8	20.6	20.6	20.5	19.6	18.7
10	20.5	20.4	20.6	20.3	20.3	20.2	19.2	18.3
20	20.1	20.1	20.1	20.0	20.0	19.8	18.9	17.9
40	19.3	19.4	19.4	19.3	19.3	19.2	18.3	17.9
80	18.9	18.9	19.0	18.9	18.9	18.7	17.8	17.4
160	18.5	18.4	18.5	18.4	18.4	18.2	17.3	16.9
320	17.5	17.4	17.4	17.4	17.4	17.3	17.0	16.4
640	17.1	17.0	16.9	16.9	16.8	16.8	16.5	15.9
1000	16.9	16.6	16.5	16.5	16.5	16.4	16.1	15.6
2000	16.4	16.4	16.4	16.4	16.4	16.2	15.8	15.1



FUNCTION DESCRIPTION

Overview

The MS5146T/MS5147T/MS5148T is highly integrated 24bit analog-to digital converter. They integrate low-noise, high input impedance programmable gain amplifier, input multiplexer, low temperature drift reference, Σ - Δ ADC, internal oscillator and SPI interface

Analog Input Channel

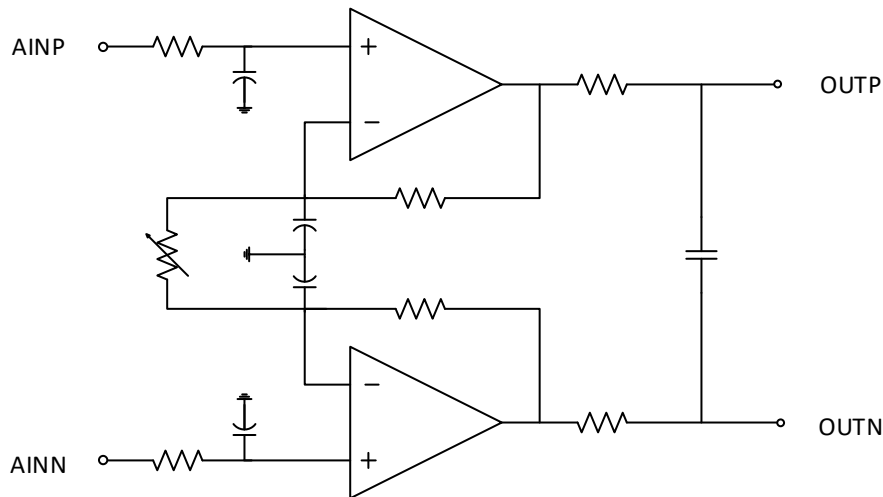
The ADC inputs are input to internal modulator through the onboard multiplexer and PGA.

The MS5146T has one pair of differential inputs. The MS5147T can be configured as two differential inputs by the MUX0 register. The MS5148T can be configured as four differential inputs by the MUX0 register. In addition, input port can be configured to connected to internal excitation circuit generator or bias voltage generator.

Temperature, AVDD, DVDD, and external reference can be detected by the input multiplexer. Input can also be configured as GPIO.

Low-noise PGA

The MS5146T/MS5147T/MS5148T integrates a programmable amplifier featured by low drift, low noise, high input impedance. Gain is set as 1, 2, 4, 8, 16, 32, 64, 128 by register SYS0. PGA consists of two chopper stable amplifiers and resistor feedback. PGA input is equipped with an electromagnetic interference filter as shown below.



The relationship between gain setting and full-scale input range is shown as follows:

$$FSR = \pm V_{REF} / GAIN$$

Common-mode input range is shown as follows:

$$V_{AVSS} + 0.1V + 0.5 \times GAIN \times V_{IN (Max)} \leq V_{CM} \leq V_{AVDD} - 0.1V - 0.5 \times GAIN \times V_{IN (Max)}$$



Clock Source

The MS5146T/MS5147T/MS5148T can use external clock or internal clock. CLK pin is connected to GND before power up or reset and internal clock is activated. Internal clock would be off when CLK pin is connected with external clock source at any time. At this time, the MS5146T/MS5147T/MS5148T would operate in the external clock mode all the time. Only when power up again or reset, it would change the operation mode in this condition.

Modulator

The MS5146T/MS5147T/MS5148T integrates third-order modulator. PCM data stream is output to digital filter. The clock rate is set as follows:

Conversion Rate (SPS)	Modulator Sample Rate (kHz)	f_{CLK}/f_{MOD}
5, 10, 20	32	128
40, 80, 160	128	32
320, 640, 1000	256	16
2000	512	8

Digital Filter

The MS5146T/MS5147T/MS5148T integrates a programmable FIR digital filter. The filtering characteristics of 4.096MHz external clock are shown below.

Nominal Conversion Rate	Actual Conversion Rate	-3dB Bandwidth	50Hz, 60Hz Rejection Characteristic			
			50Hz±0.3Hz	60Hz±0.3Hz	50Hz±1Hz	60Hz±1Hz
5SPS	5.018SPS	2.26Hz	-106dB	-74dB	-81dB	-69dB
10SPS	10.037SPS	4.76Hz	-106dB	-74dB	-80dB	-69dB
20SPS	20.075SPS	14.8Hz	-71dB	-74dB	-66dB	-68dB
40SPS	40.15SPS	9.03Hz	-	-	-	-
80SPS	80.301SPS	19.8Hz	-	-	-	-
160SPS	160.6SPS	118Hz	-	-	-	-
320SPS	321.608SPS	154Hz	-	-	-	-
640SPS	643.21SPS	495Hz	-	-	-	-
1000SPS	1000SPS	732Hz	-	-	-	-
2000SPS	2000SPS	1465Hz	-	-	-	-



Internal Reference Voltage

The MS5146T/MS5147T/MS5148T integrates a 2.048V low temperature drift reference.

2.2 μ F~47 μ F capacitor needs to be connected between VREFOUT and VREFCOM. The capacitor with larger value has better noise-filtering effect, but the turn-on time would be larger. For stability, VREFCOM needs a AC path with less than 10 Ω to AVSS. The table below shows the relationship between turn-on time and external capacitor.

VREFOUT Capacitor	Setup Error	Setup Time
2.2 μ F	$\pm 0.5\%$	150 μ s
	$\pm 0.1\%$	240 μ s
4.7 μ F	$\pm 0.5\%$	295 μ s
	$\pm 0.1\%$	376 μ s
47 μ F	$\pm 0.5\%$	2.3ms
	$\pm 0.1\%$	2.5ms

Excitation Current Output

For RTD application, the MS5147T and MS5148T integrate two matched excitation current sources (IDACs) . For three-wire RTD application, matched current source can remove the error effect caused by lead resistance. Output current source can be configured as 50 μ A, 100 μ A, 250 μ A, 500 μ A, 750 μ A, 1000 μ A, 1500 μ A.

Sensor Detection

By internal register, Burnout current is configured (0.5 μ A, 2 μ A, 10 μ A) to detect whether external sensor losses efficacy. When sensor is open circuit, Burnout current source pulls the positive input to AVDD and the negative input is pulled to AVSS, thus resulting in full-scale conversion output. A full-scale conversion output indicates that the sensor is overloaded or there is no reference voltage. A near-zero conversion output indicates the sensor is shorted circuit.

Bias Voltage Generator

For unbiased thermocouple application, the MS5146T/MS5147T/MS5148T integrates bias voltage generator. The voltage is mid-level of analog power supply. For different sensor capacitance, the setup times of bias voltage are different as shown below. When bias voltage is used on several channels, it would cause shorted circuit of internal channel. Therefore, must limit the current flowing through the device.

Sensor Capacitor	Setup Time
0.1 μ F	220 μ s
1 μ F	2.2ms
10 μ F	22ms
200 μ F	450ms



Digital General-Purpose IO

By register, analog input multiple port can be configured as analog input or GPIO. Register IOCFG control whether digital IO or not. Register IODIR controls the input and output characteristics of digital port. Register IODAT controls the definite data type of digital input and output.

Power Supply Detection

The MS5146T/MS5147T/MS5148T integrates the detection function of digital and analog power supply. The detection result is 1/4 of power supply.

External Reference Voltage Detection

The MS5146T/MS5147T/MS5148T integrates the detection function of external reference voltage. The detection result is 1/4 of actual external reference voltage. Internal reference voltage must be enabled when external reference voltage is detected.

Ambient Temperature Detection

The MS5146T/MS5147T/MS5148T integrates the detection function of ambient temperature. When temperature detection is enabled, the anodes of two diodes are connected to analog input. In room temperature, the input voltage difference is 110mV and temperature drift is 375 μ V/ $^{\circ}$ C.

Power Up

When the MS5146T/MS5147T/MS5148T is powered up, internal power-up reset circuit generates a reset pulse that resets all digital circuits. Reset time is 2^{16} system clock periods. SPI interface cannot be operated during reset. **It is recommended to perform one reset operation after power up.**

Reset

When $\overline{\text{RESET}}$ pin becomes low-level, internal reset is triggered and all registers are reset to default values. When system clock is 4.096MHz, after the rising edge on $\overline{\text{RESET}}$ pin, the chip would exit from reset state after 2ms. Chip reset can be performed by setting $\overline{\text{RESET}}$ command.

Power Down

The MS5146T/MS5147T/MS5148T uses SLEEP command or pulls START low to enter power-down mode.

Conversion Control

By START rising edge, the MS5146T/MS5147T/MS5148T can precisely control the start of conversion period. After conversion is completed, internal $\overline{\text{DRDY}}$ becomes low. When DRDY MODE bit is 1 in the IDAC0 register, DOUT/ $\overline{\text{DRDY}}$ becomes low after conversion. The chip automatically enters power-down mode when conversion is completed and START is low-level. When next START rising edge occurs, internal analog circuit needs setup time for $32 f_{\text{MOD}}$ clock period.

When START is high-level, chip would convert continuously.

Conversion can also be performed by SPI commands. Using WAKEUP command can awake one conversion. When using command control, START must be set to high. In addition, sending SYNC command can immediately start one new conversion. If writing to any of register MUX0, VBIAS, MUX1 and SYS0, digital filter would be reset and re-start one conversion correspondingly.



Single Period Setup

The MS5146T/MS5147T/MS5148T can complete single period setup for all gain and conversion rate settings. When conversion rate is 2kSPS, WREG command is used to change configuration register, SCLK period cannot exceed 520ns and the time between two near register bytes cannot exceed 4.2μs. In addition, when starting to perform several write operations to four address registers, it is necessary to wait at least 64 system clock periods before performing write commands.

Digital Filter Reset Operation

Digital filter would be reset when the MS5146T/MS5147T/MS5148T performs following operations: send RESET command; write to register MUX0, VBIAS, MUX1, SYS0; send SYNC command and rising edge occurs on START pin.

Calibration

Offset calibration and gain calibration are performed before conversion result is output. The conversion result of ADC is first subtracted by zero-scale calibration value (OFC register) and then is multiplied by gain calibration coefficient.

$$\text{Output Data} = (\text{Input} - \text{OFC}[2:0]) \times \frac{\text{FSC}[2:0]}{400000h}$$

Calibration Command

The MS5146T/MS5147T/MS5148T provides three calibration commands: system gain calibration, system offset calibration and offset self-calibration.

System Offset and Offset Self-Calibration

System offset calibration can calibrate the internal and external offset errors. System offset calibration can be initiated by sending SYSOCAL command. Offset self-calibration can be initiated by sending SELFOCAL command. During offset self-calibration, the configured input channel is disconnected from the external circuit, connecting the inputs to mid value of power supply. OFC register is updated after the conversion is completed.

System Gain Calibration

The gain error on the path of system gain calibration signal can be activated by sending SYSGCAL command.

Calibration Time

After calibration is activated, 16 corresponding conversions are performed. Then average the conversion result and calculate calibration value, which can improve the calibration precision. The calibration time is shown as follows:

$$\text{Calibration Time} = 50/f_{\text{CLK}} + 30/f_{\text{MOD}} + 16/f_{\text{DATA}}$$



Digital Interface

The MS5146T/MS5147T/MS5148T provides serial communication interface compatible with SPI and data ready signal.

$\overline{\text{CS}}$

The $\overline{\text{CS}}$ pin activates SPI communication. $\overline{\text{CS}}$ must be low before data transmission and during SPI communication period. When $\overline{\text{CS}}$ is high, DOUT/ $\overline{\text{DRDY}}$ pin enters a high-impedance state. Therefore, the serial interface would be reset and reading and writing are ignored at this time. $\overline{\text{DRDY}}$ pin is independent of $\overline{\text{CS}}$. Even though $\overline{\text{CS}}$ is high, $\overline{\text{DRDY}}$ still indicates that a new conversion has completed and is forced high after SCLK response.

Setting $\overline{\text{CS}}$ high only disables SPI communication. Data conversion and data ready function can still continue operating.

SCLK

SCLK is the clock for serial communication. Data is input into DIN on the falling edge of SCLK and output from DOUT on the rising edge of SCLK.

DIN

Data is input into DIN on the falling edge of SCLK. Even though data is read out, the chip also can recognize written command. Therefore, during reading data, if not send other commands to the chip at the same time, please send NOP command on DIN.

$\overline{\text{DRDY}}$

$\overline{\text{DRDY}}$ pin low indicates a new conversion is completed, and the conversion result is stored in the buffer. SCLK must remain low for t_{DTS} after $\overline{\text{DRDY}}$ becomes low, so that the conversion result is loaded into the buffer and output shift register. After $\overline{\text{DRDY}}$ pin becomes low, it is forced high on the first falling edge of SCLK. If $\overline{\text{DRDY}}$ pin is not set to high by the clock signal on SCLK after it becomes low, a high pulse for t_{PWH} would be generated when new data is ready.

DOUT/ $\overline{\text{DRDY}}$

DOUT/ $\overline{\text{DRDY}}$ pin has two modes: only data out (DOUT) or DOUT with data ready ($\overline{\text{DRDY}}$). DRDY MODE bit determines the function of this pin. When $\overline{\text{CS}}$ is high, DOUT/ $\overline{\text{DRDY}}$ pin becomes high-impedance state.

When DRDY MODE bit is set to 0, this pin is only as DOUT. Data is read out on the rising edge of SCLK, MSB first.

When DRDY MODE bit is set to 1, this pin has functions for DOUT and $\overline{\text{DRDY}}$. The mode is invalid when the chip is in stop read data continuous mode.

DRDY MODE only acts on DOUT/ $\overline{\text{DRDY}}$ pin and has no influence on $\overline{\text{DRDY}}$ pin.

When DRDY MODE bit is set to 1 and a new conversion is completed, DOUT/ $\overline{\text{DRDY}}$ becomes low if it is high. If DOUT/ $\overline{\text{DRDY}}$ is low, it would first become high and then become low. Similar to $\overline{\text{DRDY}}$ pin, the falling edge signal on the DOUT/ $\overline{\text{DRDY}}$ pin indicates that new conversion result is ready. When data is read out, only can send NOP command or other commands which cannot load data output register. DOUT/ $\overline{\text{DRDY}}$ pin would become high after the first rising edge of SCLK after reading the conversion result.



SPI Reset

By pulling \overline{CS} pin high, only reset the serial interface without resetting the registers and digital filter. Pulling \overline{RESET} pin low can reset the serial interface and all digital functions and start a new conversion.

When \overline{CS} remains low all the time, completed 8bit as a byte, must be written to register. Otherwise, SPI communication would be abnormal and the chip cannot recognize commands. If the idle time of SPI for 64 conversion periods, the interface would be reset.

SPI Communication in Power-down Mode

When START pin is low or the chip is in power-down mode, can only send the following commands: RDATA, RDATAc, SDTAC, WAKEUP and NOP. RDATA command can be used to repeatedly read last conversion result.

Data Format

The output data format is 24bit binary complement. The calculation formula of LSB is shown as follows:

$$1 \text{ LSB} = (2 \times V_{\text{REF}} / \text{Gain}) / 2^{24} = +\text{FS} / 2^{23}$$

Positive full-scale input (FS) [$V_{\text{IN}} \geq (+\text{FS} - 1 \text{ LSB}) = (V_{\text{REF}} / \text{Gain} - 1 \text{ LSB})$] has output code 7FFFFFFh. Negative full-scale input ($V_{\text{IN}} \leq -\text{FS} = -V_{\text{REF}} / \text{Gain}$) has output code 800000h. The table below shows the ideal output code of different input signals.

Input V_{IN} ($\text{AIN}_P - \text{AIN}_N$)	Ideal Output Code
$\geq \text{FS} (2^{23} - 1) / 2^{23}$	7FFFFFFh
$\text{FS} / 2^{23}$	000001h
0	000000h
$-\text{FS} / 2^{23}$	FFFFFFh
$\leq -\text{FS}$	800000h

Command

The MS5146T/MS5147T/MS5148T can be controlled by 13 commands. For RREG and WREG commands, there needs extra byte to be as a part of command. NOP command can be used to read chip data and other commands are not sent at the same time.

1. n = Number of Read/Write Register - 1;
2. r = Register Address;
3. x = Don't care.

Command	Description	First Command Byte	Second Command Byte
WAKEUP	Exit from Power-down Mode	0000 000x(00h,01h)	
SLEEP	Enter into Power-down Mode	0000 001x(02h,03h)	
SYNC	Synchronous ADC Conversion	0000 010x(04h,05h)	0000 010x(04,05h)
\overline{RESET}	Reset	0000 011x(06h,07h)	
NOP	No Operation	1111 1111(FFh)	
READ_DATA	Single Read Data	0001 001x(12h,13h)	



Command	Description	First Command Byte	Second Command Byte
READ_DATA	Continuous Read Rata	0001 010x(14h,15h)	
STOP_DATA	Stop Continuous Read Rata	0001 011x(16h,17h)	
READ_REG	Read Register rrrr	0010 rrrr(2xh)	0000 nnnn
WRITE_REG	Write Register rrrr	0100 rrrr(4xh)	0000 nnnn
SYS_OFFSETCAL	System Offset Calibration	0110 0000(60h)	
SYS_GAINCAL	System Gain Calibration	0110 0001(61h)	
SELF_OFFSETCAL	Internal Offset Calibration	0110 0010(62h)	
RESTRICTED	Restricted Command	1111 0001(F1h)	

WAKEUP (0000 000x)

After performing SLEEP command, the chip is powered up by WAKEUP command. After performing WAKEUP command, the chip would be powered up on the eighth falling edge of SCLK.

SLEEP (0000 001x)

After sending SLEEP command, the chip enters into power-down mode after it completes current conversion. Note that this command wouldn't turn off internal reference voltage.

Single conversion can be performed after sending WAKEUP command followed by SLEEP command.

WAKEUP and SLEEP commands are equivalent of the control of START pin.

If START pin is low-level, WAKEUP command is invalid. When SLEEP command takes effect, \overline{CS} must hold low-level.

SYNC (0000 010x)

SYNC command would reset ADC digital filter. By sending SYNC command, several devices can be synchronously connected to same SPI bus.

RESET (0000 011x)

Reset command can reset all registers and digital filter. The command is equivalent of \overline{RESET} pin. However, RESET command cannot reset serial interface. Serial interface can be reset by \overline{CS} pin and then the chip is reset by sending RESET command. RESET command is similar to hardware reset. When system clock frequency is 4.096MHz, there needs 2ms to reset. Therefore, after sending RESET command, must wait for 2ms, then SPI communication starts again.

READ_DATA (0001 001x)

READ_DATA command can load the most recent conversion result into output register. In READ_DATA mode, the command can also take effect.

When reading conversion result more than once, the command is sent at last 8 clocks when reading the last conversion result.



READ_DATAC (0001 010x)

READ_DATAC command enables the continuous read data mode. This mode is the default mode after power-up reset. In continuous read data mode, new conversion result would be automatically loaded into DOUT. The conversion result can be read from the chip by sending 24 SCLKs after $\overline{\text{DRDY}}$ goes low. READ_DATAC command must be sent after $\overline{\text{DRDY}}$ goes low, and takes effect on the next $\overline{\text{DRDY}}$.

Be sure to complete data read (conversion result or register readback) before $\overline{\text{DRDY}}$ returns low, otherwise data would be lost.

STOP_DATAC (0001 011x)

STOP_DATAC command stops the continuous read data mode. In stop continuous read data mode, the conversion result would not be automatically loaded into DOUT when $\overline{\text{DRDY}}$ goes low. In this mode, reading the chip wouldn't be interrupted when new ADC conversion is completed. And use READ_DATA command to get conversion result. STOP_DATAC command takes effect when next $\overline{\text{DRDY}}$ goes low.

READ_REG (0010 rrrr, 0000 nnnn)

By READ_REG command, 15 groups of registers can be read. The number of read registers equals to one plus the value of second command byte. If the count exceeds the remaining registers, the addresses would return to initial position. The two-byte command structure for READ_REG is shown as follows.

1. First Command Byte: 0010 rrrr, rrrr is the register address of first read;
2. Second Command Byte: 0000 nnnn, nnnn=the number of register to read -1.

WRITE_REG (0100 rrrr, 0000 nnnn)

By WRITE_REG command, 15 groups of registers can be written. The number of write registers equals to one plus the value of second command byte. The two-byte command structure for WRITE_REG is shown as follows.

1. First Command Byte: 0100 rrrr, rrrr is the register address of first write;
2. Second Command Byte: 0000 nnnn, nnnn=the number of register to write -1.

SYS_OFFSETCAL (0110 0000)

SYS_OFFSETCAL command initiates the system offset calibration. For system offset calibration, analog input must be externally shorted to the voltage within the input common-mode range. Analog input should be near the value of $(V_{\text{AVDD}} + V_{\text{AVSS}})/2$. OFC register would be automatically updated when this command is completed.

SYS_GAINCAL (0110 0001)

SYS_GAINCAL command initiates the system gain calibration. For system gain calibration, analog input must be set to full-scale. FSC register would be automatically updated when this command is completed.

SELF_OFFSETCAL (0110 0010)

SELF_OFFSETCAL command initiates the system offset calibration. For system offset calibration, analog input is internally shorted to mid-supply and calibration is performed. OFC register would be automatically updated when this command is completed.



NOP (1111 1111)

No operation command.

RESTRICTED

The command is restricted to send to chip.

Register Address Map
MS5146T Register Address Map

Address	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00h	BCS	BCS[1:0]		0	0	0	0	0	1
01h	VBIAS	0	0	0	0	0	0	VBIAS[1:0]	
02h	MUX1	CLKSATA	0	0	0	0	MUXCAL[2:0]		
03h	SYS0	0	PGA[2:0]			DR[3:0]			
04h	OFC0	OFC[7:0]							
05h	OFC1	OFC[15:8]							
06h	OFC2	OFC[23:16]							
07h	FSC0	FSC[7:0]							
08h	FSC1	FSC[15:8]							
09h	FSC2	FSC[23:16]							
0Ah	ID	ID[3:0]				DRDY MODE	0	0	0

BCS: Burnout Current Source Register

Address=00h; Reset Value=01h

Bit	Name	Type	Reset Value	Description
7:6	BCS[1:0]	R/W	0h	Burnout current source detection, control current source: 00: Burnout current off (default); 01: Burnout current on, 0.5μA; 10: Burnout current on, 2μA; 11: Burnout current on, 10μA.
5:0	Reserved	R	01h	000001.



VBIAS: Bias Voltage Register
Address=01h; Reset Value=01h

Bit	Name	Type	Reset Value	Description
7:2	Reserved	R	00h	000000.
1	VBIAS[1]	R/W	0h	AINN bias voltage enable, apply the bias voltage of (AVDD +AVSS) / 2 to AINN: 0: Disable bias voltage (default); 1: Enable bias voltage.
0	VBIAS[0]	R/W	0h	AINP bias voltage enable, apply the bias voltage of (AVDD +AVSS) / 2 to AINP: 0: Disable bias voltage (default); 1: Enable bias voltage.

MUX: Multi-function Control Register
Address=02h; Reset Value=x0h

Bit	Name	Type	Reset Value	Description
7	CLKSTAT	R	xh	Clock State: 0: Internal clock is in use; 1: External clock is in use.
6:3	Reserved	R	0h	0000.
0	MUXCAL	R/W	0h	System Monitor Control Select: 000: Normal mode (default); 001: Offset calibration; 010: Gain calibration; 011: Temperature sensor.

The table below shows the internal connection in ADC and PGA setting for each MUXCAL setting.

MUXCAL[2:0]	PGA Gain Setting	ADC Analog Input
000	Set by SYS0 register	Normal mode.
001	Set by SYS0 register	Offset calibration: input is shorted to (AVDD +AVSS) / 2.
010	Forced to 1	Gain calibration: $V_{(REFP)} - V_{(REFN)}$ (full-scale).
011	Forced to 1	Temperature sensor

SYS0: System Control Register 0
Address=03h; Reset Value=00h

Bit	Name	Type	Reset Value	Description
7	Reserved	R	0h	0.
6:4	PGA[2:0]	R/W	0h	PGA Gain Setting: 000: PGA = 1 (default);



				001: PGA = 2; 010: PGA = 4; 011: PGA = 8; 100: PGA = 16; 101: PGA = 32; 110: PGA = 64; 111: PGA = 128.
0	DR[3:0]	R/W	0h	Data Output Rate Setting: 0000: DR = 5 SPS (default); 0001: DR = 10 SPS; 0010: DR = 20 SPS; 0011: DR = 40 SPS; 0100: DR = 80 SPS; 0101: DR = 160 SPS; 0110: DR = 320 SPS; 0111: DR = 640 SPS; 1000: DR = 1000 SPS; 1001 to 1111: DR = 2000 SPS.

OFC: Offset Calibration Register
Address=04h, 05h, 06h; Reset Value=000000h

Bit	Name	Type	Reset Value	Description
23:0	OFC[23:0]	R/W	000000h	Offset Calibration Coefficient Register. The ADC subtracts the register value from the conversion result before gain calibration.

Offset calibration value is complement format. The maximum positive value is 7FFFFFFh and the maximum negative value is 800000h. Note that it should be avoided that analog input exceeds the range even though the calibration range of offset calibration register is from -FS to +FS (as shown below).

Offset Calibration Register	Final Output Code at $V_{IN} = 0$
7FFFFFFh	800000h
000001h	FFFFFFh
000000h	000000h
FFFFFFh	000001h
800000h	7FFFFFFh



FSC: Gain Calibration Register
Address=07h, 08h, 09h; Reset Value=xxxxxxh

For each PGA setting, the reset value of FSC is factory setting. When PGA setting is changed, FSC would automatically load the corresponding reset value.

Bit	Name	Type	Reset Value	Description
23:0	FSC[23:0]	R/W	xxxxxxh	Gain Calibration Coefficient Register. The ADC divides the register value by 400000h to be as scale coefficient. After offset calibration, the ADC multiplies the scale coefficient by the conversion result.

Gain calibration value is unsigned binary format. When the value is 400000h, the coefficient is 1.0. Note that it should be avoided that analog input exceeds the range even though gain calibration register can calibrate the gain error more than 1 (as shown below).

Gain Calibration Register	Gain Coefficient
800000h	2.0
400000h	1.0
200000h	0.5
000000h	0

ID: ID Register
Address=0Ah; Reset Value=x0h

Bit	Name	Type	Reset Value	Description
7:4	ID[3:0]	R	xh	ID Bit.
3	DRDY MODE	R/W	0h	Data Ready Mode Setting: 0: DOUT/ <u>DRDY</u> pin is only used for data output (default); 1: DOUT/ <u>DRDY</u> pin is both used for data output and data ready, active low.
2:0	Reserved	R	0h	000.



MS5147T and MS5148T Register Map

Address	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00h	MUX0	BCS[1:0]		MUX_SP[2:0]			MUX_SN[2:0]		
01h	VBIAS	VBIAS[7:0]							
02h	MUX1	CLKSTAT	VREFCON[1:0]		REFSELT[1:0]		MUXCAL[2:0]		
03h	SYS0	0	PGA[2:0]			DR[3:0]			
04h	OFC0	OFC[7:0]							
05h	OFC1	OFC[15:8]							
06h	OFC2	OFC[23:16]							
07h	FSC0	FSC[7:0]							
08h	FSC1	FSC[15:8]							
09h	FSC2	FSC[23:16]							
0Ah	IDAC0	ID[3:0]				DRDY MODE	IMAG[2:0]		
0Bh	IDAC1	I1DIR[3:0]				I2DIR[3:0]			
0Ch	GPIOCFG	IOCFG[7:0]							
0Dh	GPDIR	IODIR[7:0]							
0Eh	GPIDAT	IODAT[7:0]							

MUX0: Multi-function Control Register 0
Address=00h; Reset Value=01h

Bit	Name	Type	Reset Value	Description
7:6	BCS[1:0]	R/W	0h	Burnout current source detection, control current source: 00: Burnout current off (default); 01: Burnout current on, 0.5μA; 10: Burnout current on, 2μA; 11: Burnout current on, 10μA.
5:3	MUX_SP[2:0]	R/W	0h	ADC Positive Input Channel Select: 000: AIN0 (default); 001: AIN1; 010: AIN2; 011: AIN3; 100: AIN4 (only MS5148T); 101: AIN5 (only MS5148T); 110: AIN6 (only MS5148T); 111: AIN7 (only MS5148T).



Bit	Name	Type	Reset Value	Description
2:0	MUX_SN[2:0]	R/W	1h	ADC Negative Input Channel Select: 000: AIN0; 001: AIN1 (default); 010: AIN2; 011: AIN3; 100: AIN4 (only MS5148T); 101: AIN5 (only MS5148T); 110: AIN6 (only MS5148T); 111: AIN7 (only MS5148T).

VBIAS: Bias Voltage Register
Address=01h; Reset Value=00h

Bit	Name	Type	Reset Value	Description
7	VBIAS[7]	R/W	0h	AIN7 bias voltage enable, apply the bias voltage of (AVDD + AVSS) / 2 to AIN7 (only MS5148T): 0: Disable bias voltage; 1: Enable bias voltage.
6	VBIAS[6]	R/W	0h	AIN6 bias voltage enable, apply the bias voltage of (AVDD + AVSS) / 2 to AIN6 (only MS5148T): 0: Disable bias voltage; 1: Enable bias voltage.
5	VBIAS[5]	R/W	0h	AIN5 bias voltage enable, apply the bias voltage of (AVDD + AVSS) / 2 to AIN5 (only MS5148T): 0: Disable bias voltage; 1: Enable bias voltage.
4	VBIAS[4]	R/W	0h	AIN4 bias voltage enable, apply the bias voltage of (AVDD + AVSS) / 2 to AIN4 (only MS5148T): 0: Disable bias voltage; 1: Enable bias voltage.
3	VBIAS[3]	R/W	0h	AIN3 bias voltage enable, apply the bias voltage of (AVDD + AVSS) / 2 to AIN3 (only MS5147T/MS5148T): 0: Disable bias voltage; 1: Enable bias voltage.
2	VBIAS[2]	R/W	0h	AIN2 bias voltage enable, apply the bias voltage of (AVDD + AVSS) / 2 to AIN2 (only MS5147T/MS5148T): 0: Disable bias voltage; 1: Enable bias voltage.



Bit	Name	Type	Reset Value	Description
1	VBIAS[1]	R/W	0h	AIN1 bias voltage enable, apply the bias voltage of (AVDD +AVSS) / 2 to AIN1: 0: Disable bias voltage; 1: Enable bias voltage.
0	VBIAS[0]	R/W	0h	AIN0 bias voltage enable, apply the bias voltage of (AVDD +AVSS) / 2 to AIN0. 0: Disable bias voltage; 1: Enable bias voltage.

MUX1: Multi-function Control Register 1
Address=02h; Reset Value=x0h

Bit	Name	Type	Reset Value	Description
7	CLKSTAT	R	xh	Clock State: 0: Internal clock is in use; 1: External clock is in use.
6:5	VREFCON[1:0]	R/W	0h	Internal Reference Control Bit: 00: Internal reference is always off (default); 01: Internal reference is always on; 10 or 11: Internal reference is on in normal operation mode. Internal reference is off in power-down mode.
4:3	REFSELT[1:0]	R/W	0h	Reference Select: 00: Select external reference, input from REFPO and REFNO pins (default); 01: Select external reference, input from REFP1 and REFN1 pins (only MS5148T); 10: Select internal reference; 11: Select internal reference, output to REFPO and REFNO pins.
2:0	MUXCAL[2:0]	R/W	0h	System Monitor Control Select: 000: Normal mode (default); 001: Offset calibration; 010: Gain calibration; 011: Temperature sensor; 100: Monitor REF1 (only MS5148T); 101: Monitor REF0; 110: Monitor Analog Power; 111: Monitor Digital Power.



The table below shows the internal connection in ADC and PGA setting for each MUXCAL setting.

MUXCAL[2:0]	PGA Gain Setting	ADC Analog Input
000	Set by SYS0 register	Normal mode
001	Set by SYS0 register	Input shorted to (AVDD +AVSS) / 2
010	Forced to 1	$V_{(REFP)} - V_{(REFN)}$ (full-scale)
011	Forced to 1	Temperature sensor
100	Forced to 1	$V_{(REFP1)} - V_{(REFN1)} / 4$
101	Forced to 1	$V_{(REFP0)} - V_{(REFN0)} / 4$
110	Forced to 1	(AVDD - AVSS) / 4
111	Forced to 1	(DVDD - DGND) / 2

SYS0: System Control Register 0

Address=03h; Reset Value=00h

Bit	Name	Type	Reset Value	Description
7	Reserved	R	0h	0.
6:4	PGA[2:0]	R/W	0h	PGA Gain Setting: 000: PGA = 1 (default); 001: PGA = 2; 010: PGA = 4; 011: PGA = 8; 100: PGA = 16; 101: PGA = 32; 110: PGA = 64; 111: PGA = 128.
0	DR[3:0]	R/W	0h	Data Output Rate Setting: 0000: DR = 5 SPS (default); 0001: DR = 10 SPS; 0010: DR = 20 SPS; 0011: DR = 40 SPS; 0100: DR = 80 SPS; 0101: DR = 160 SPS; 0110: DR = 320 SPS; 0111: DR = 640 SPS; 1000: DR = 1000 SPS; 1001 to 1111: DR = 2000 SPS.



OFC: Offset Calibration Register
Address=04h, 05h, 06h; Reset Value=000000h

Bit	Name	Type	Reset Value	Description
23:0	OFC[23:0]	R/W	000000h	Offset Calibration Coefficient Register. The ADC subtracts the register value from the conversion result before gain calibration.

Offset calibration value is complement format. The maximum positive value is 7FFFFFFh and the maximum negative value is 800000h. Note that it should be avoided that analog input exceeds the range even though the calibration range of offset calibration register is from -FS to +FS (as shown below).

Offset Calibration Register	Final Output Code at $V_{IN} = 0$
7FFFFFFh	800000h
000001h	FFFFFFh
000000h	000000h
FFFFFFh	000001h
800000h	7FFFFFFh

FSC: Gain Calibration Register
Address=07h, 08h, 09h; Reset Value =xxxxxxh

For each PGA setting, the reset value of FSC is factory setting. When PGA setting is changed, FSC would automatically load the corresponding reset value.

Bit	Name	Type	Reset Value	Description
23:0	FSC[23:0]	R/W	xxxxxxh	Gain Calibration Coefficient Register. The ADC divides the register value by 400000h to be as scale coefficient. After offset calibration, the ADC multiplies the scale coefficient by the conversion result.

Gain calibration value is unsigned binary format. When the value is 400000h, the coefficient is 1.0. Note that it should be avoided that analog input exceeds the range even though gain calibration register can calibrate the gain error more than 1 (as shown below).

Gain Calibration Register	Gain Coefficient
800000h	2.0
400000h	1.0
200000h	0.5
000000h	0



IDAC0: IDAC Control Register 0
Address=0Ah; Reset Value=x0h

Bit	Name	Type	Reset Value	Description
7:4	ID[3:0]	R	xh	ID Bit.
3	DRDY MODE	R/W	0h	Data Ready Mode Setting: 0: DOUT/ $\overline{\text{DRDY}}$ pin is only used for data output (default); 1: DOUT/ $\overline{\text{DRDY}}$ pin is both used for data output and data ready, active low.
2:0	IMAG[2:0]	R/W	0h	IDAC Excitation Current: 000: Off (default); 001: 50 μA ; 010: 100 μA ; 011: 250 μA ; 100: 500 μA ; 101: 750 μA ; 110: 1000 μA ; 111: 1500 μA .

IDAC1: IDAC Control Register 1
Address=0Bh; Reset Value=FFh

Bit	Name	Type	Reset Value	Description
7:4	I1DIR[3:0]	R/W	Fh	IDAC Excitation Current Output Channel 1: 0000: AIN0; 0001: AIN1; 0010: AIN2; 0011: AIN3; 0100: AIN4 (only MS5148T); 0101: AIN5 (only MS5148T); 0110: AIN6 (only MS5148T); 0111: AIN7 (only MS5148T); 10x0: IEXC1 (only MS5148T); 10x1: IEXC2 (only MS5148T); 11xx: Not connection (default).
3:0	I2DIR[3:0]	R/W	Fh	IDAC Excitation Current Output Channel 2: 0000: AIN0; 0001: AIN1; 0010: AIN2; 0011: AIN3; 0100: AIN4 (only MS5148T); 0101: AIN5 (only MS5148T); 0110: AIN6 (only MS5148T);



				0111: AIN7 (only MS5148T); 10x0: IEXC1 (only MS5148T); 10x1: IEXC2 (only MS5148T); 11xx: Not connection (default).
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GPIOCFG: GPIO Configuration Register
Address=0Ch; Reset Value=00h

Bit	Name	Type	Reset Value	Description
7	IOCFG[7]	R/W	0h	GPIO7 (AIN7) Pin Configuration (only MS5148T): 0: GPIO[7] is disabled (default); 1: GPIO[7] is applied to AIN7.
6	IOCFG[6]	R/W	0h	GPIO[6] (AIN6) Pin Configuration (only MS5148T): 0: GPIO[6] is disabled (default); 1: GPIO[6] is applied to AIN6.
5	IOCFG[5]	R/W	0h	GPIO[5] (AIN5) Pin Configuration (only MS5148T): 0: GPIO[5] is disabled (default); 1: GPIO[5] is applied to AIN5.
4	IOCFG[4]	R/W	0h	GPIO[4] (AIN4) Pin Configuration (only MS5148T): 0: GPIO[4] is disabled (default); 1: GPIO[4] is applied to AIN4.
3	IOCFG[3]	R/W	0h	GPIO[3] (AIN3) Pin Configuration: 0: GPIO[3] is disabled (default); 1: GPIO[3] is applied to AIN3.
2	IOCFG[2]	R/W	0h	GPIO[2] (AIN2) Pin Configuration: 0: GPIO[2] is disabled (default); 1: GPIO[2] is applied to AIN2.
1	IOCFG[1]	R/W	0h	GPIO[1] (REFN0) Pin Configuration: 0: GPIO[1] is disabled (default); 1: GPIO[1] is applied to REFN0.
0	IOCFG[0]	R/W	0h	GPIO[0] (REFP0) Pin Configuration: 0: GPIO[0] is disabled (default); 1: GPIO[0] is applied to REFP0.



GPIODIR: GPIO Direction Register
Address=0Dh; Reset Value=00h

Bit	Name	Type	Reset Value	Description
7	IODIR[7]	R/W	0h	GPIO[7] (AIN7) Pin Direction (only MS5148T): 0: GPIO[7] as output pin (default); 1: GPIO[7] as input pin.
6	IODIR[6]	R/W	0h	GPIO[6] (AIN6) Pin Direction (only MS5148T): 0: GPIO[6] as output pin (default); 1: GPIO[6] as input pin.
5	IODIR[5]	R/W	0h	GPIO[5] (AIN5) Pin Direction (only MS5148T): 0: GPIO[5] as output pin (default); 1: GPIO[5] as input pin.
4	IODIR[4]	R/W	0h	GPIO[4] (AIN4) Pin Direction (only MS5148T): 0: GPIO[4] as output pin (default); 1: GPIO[4] as input pin.
3	IODIR[3]	R/W	0h	GPIO[3] (AIN3) Pin Direction: 0: GPIO[3] as output pin (default); 1: GPIO[3] as input pin.
2	IODIR[2]	R/W	0h	GPIO[2] (AIN2) Pin Direction: 0: GPIO[2] as output pin (default); 1: GPIO[2] as input pin.
1	IODIR[1]	R/W	0h	GPIO[1] (REFN0) Pin Direction: 0: GPIO[1] as output pin (default); 1: GPIO[1] as input pin.
0	IODIR[0]	R/W	0h	GPIO[0] (REFP0) Pin Direction: 0: GPIO[0] as output pin (default); 1: GPIO[0] as input pin.



GPIODAT: GPIO Data Register
Address=0Eh; Reset Value=00h

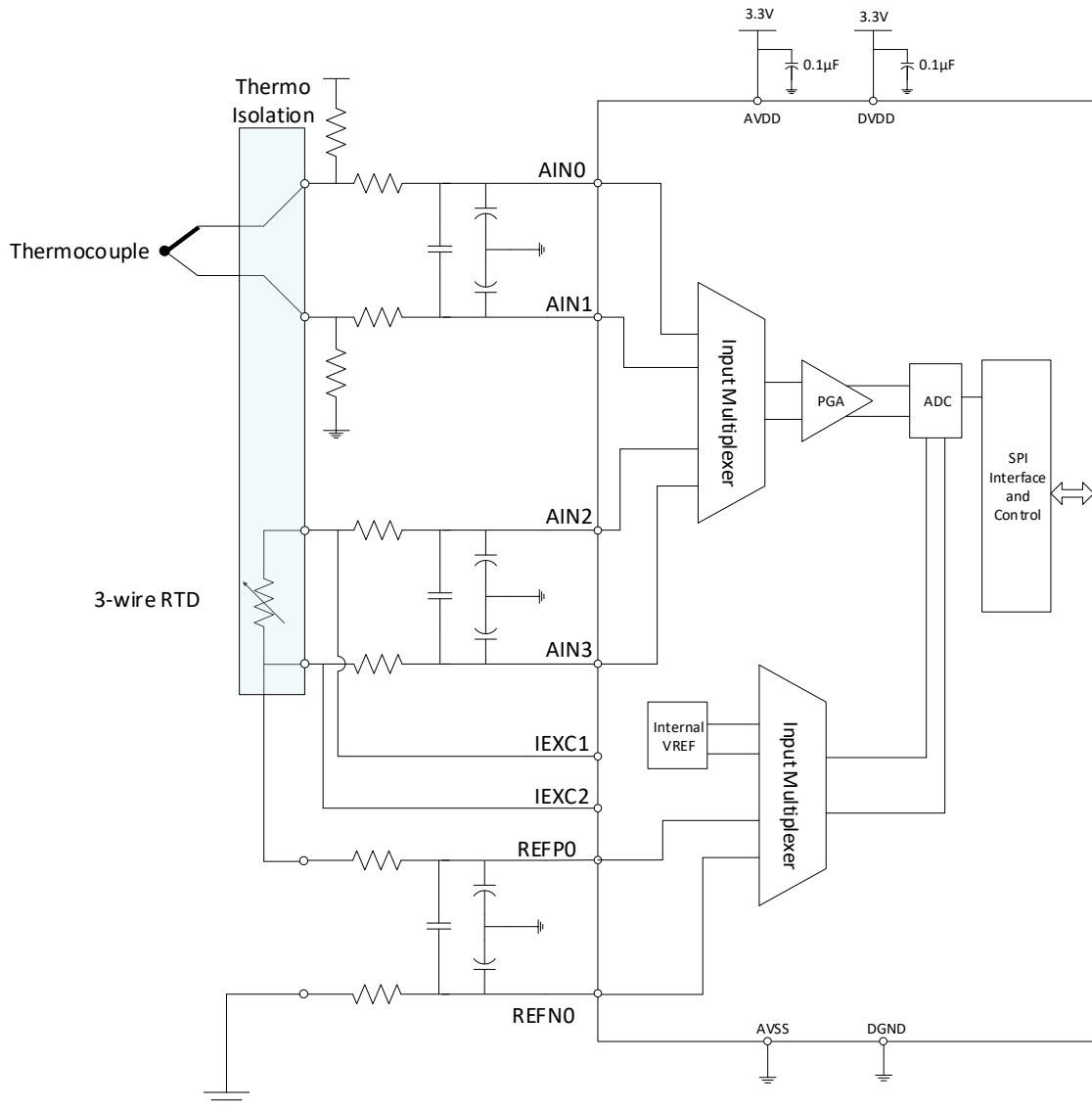
When corresponding pin is configured as output pin, the register value can be readback. When corresponding pin is configured as input pin, writing to register can only change the value, but cannot output to corresponding pin.

Bit	Name	Type	Reset Value	Description
7	IODAT[7]	R/W	0h	GPIO[7] (AIN7) Pin Data (only MS5148T); 0: GPIO[7] low (default); 1: GPIO[7] high.
6	IODAT[6]	R/W	0h	GPIO[6] (AIN6) Pin Data (only MS5148T); 0: GPIO[6] low (default); 1: GPIO[6] high.
5	IODAT[5]	R/W	0h	GPIO[5] (AIN5) Pin Data (only MS5148T); 0: GPIO[5] low (default); 1: GPIO[5] high.
4	IODAT[4]	R/W	0h	GPIO[4] (AIN4) Pin Data (only MS5148T); 0: GPIO[4] low (default); 1: GPIO[4] high.
3	IODAT[3]	R/W	0h	GPIO[3] (AIN3) Pin Data: 0: GPIO[3] low (default); 1: GPIO[3] high.
2	IODAT[2]	R/W	0h	GPIO[2] (AIN2) Pin Data: 0: GPIO[2] low (default); 1: GPIO[2] high.
1	IODAT[1]	R/W	0h	GPIO[1] (REFN0) Pin Data: 0: GPIO[1] low (default); 1: GPIO[1] high.
0	IODAT[0]	R/W	0h	GPIO[0] (REFP0) Pin Data: 0: GPIO[0] low (default); 1: GPIO[0] high.



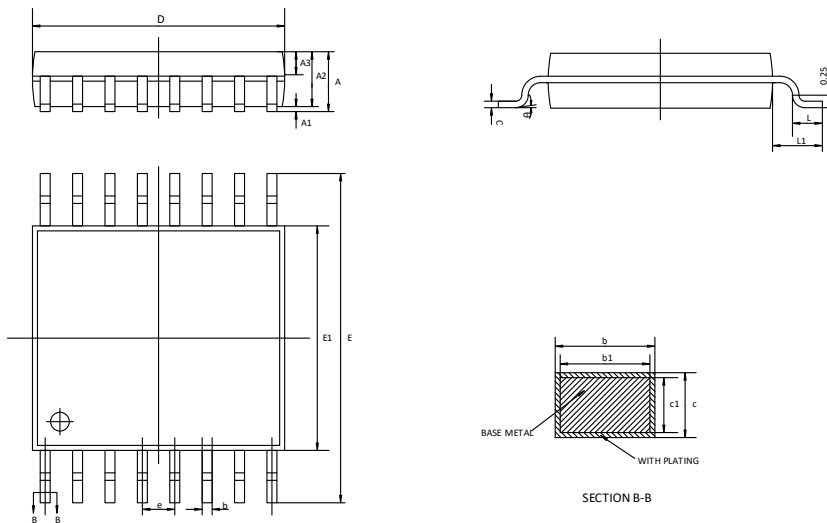
TYPICAL APPLICATION DIAGRAM

The figure below shows the thermocouple measurement application for the MS5148T



PACKAGE OUTLINE DIMENSIONS

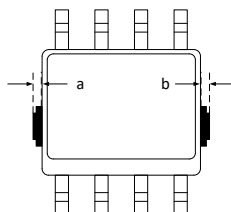
TSSOP16



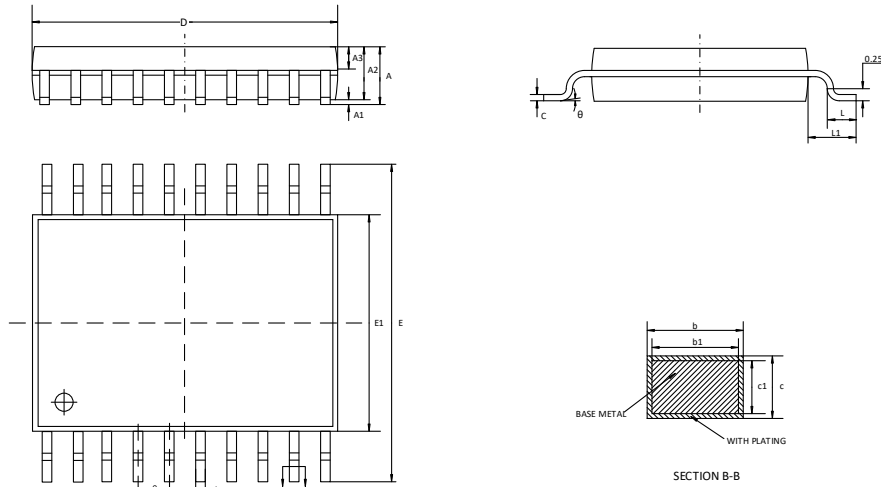
Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0°	-	8°

Note: In addition to the package size, a, b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.

The diagram is as follows: taking SOP8 package as an example.



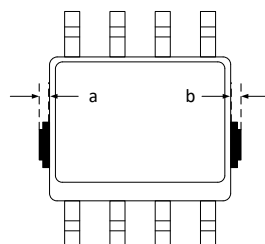
TSSOP20



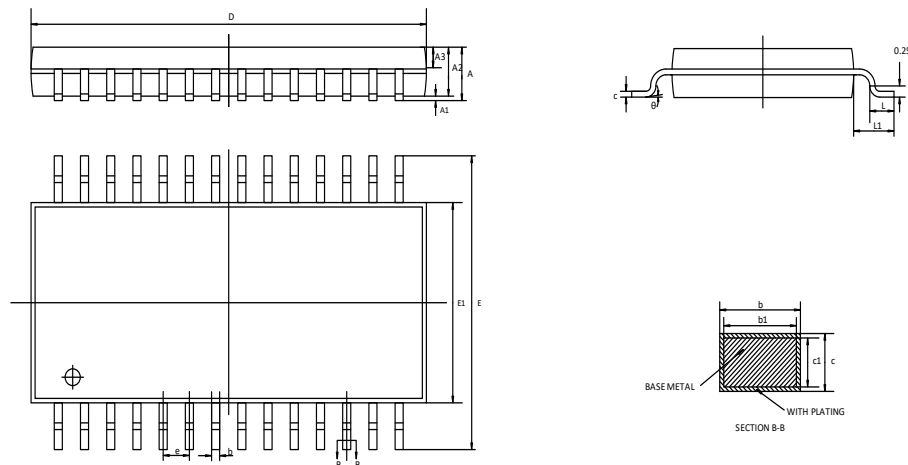
Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	-	8°

Note: In addition to the package size, a, b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.

The diagram is as follows: taking SOP8 package as an example.



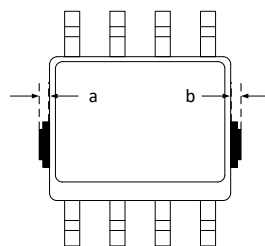
TSSOP28



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.00
A3	0.39	0.44	0.49
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.14	-	0.18
c1	0.12	0.13	0.14
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0°	-	8°

Note: In addition to the package size, a, b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.

The diagram is as follows: taking SOP8 package as an example.



MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: MS5146T, MS5147T, MS5148T

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS5146T	TSSOP16	3000	1	3000	8	24000
MS5147T	TSSOP20	3000	1	3000	8	24000
MS5148T	TSSOP28	3000	1	3000	8	24000



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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.



**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

