

100V N+P-Channel Enhancement Mode MOSFET

Description

The AP8G06NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 100V$ $I_D = 8A$

$R_{DS(ON)} < 75m\Omega$ @ $V_{GS}=10V$

$V_{DS} = -100V$ $I_D = -6.5A$

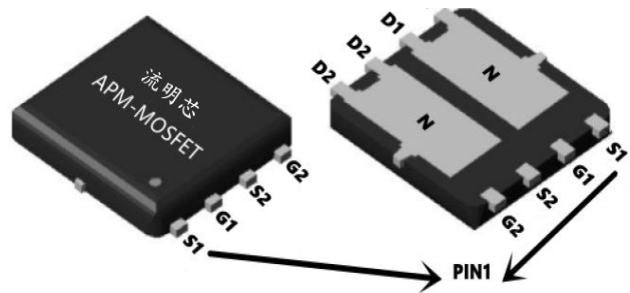
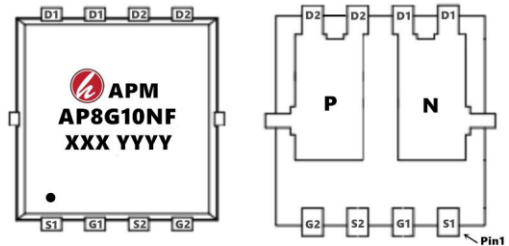
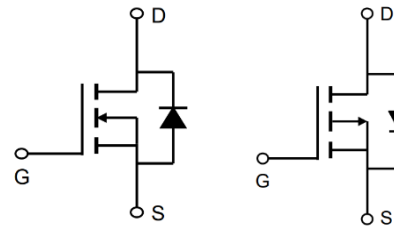
$R_{DS(ON)} < 210m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP8G10NF	PDFN5*6-8L	AP8G10NF XXX YYYY	5000

Absolute Maximum Ratings at $T_J=25^\circ C$ unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain source voltage	V_{DS}	100	-100V	V
Gate source voltage	V_{GS}	± 20	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ C$	I_D	8	-6.5	A
Pulsed drain current ²⁾ , $T_C=25^\circ C$	I_D , pulse	45	-40	A
Power dissipation ³⁾ , $T_C=25^\circ C$	P_D	17	54	W
Single pulsed avalanche energy ⁴⁾	EAS	4.2	38	mJ
Operation and storage temperature	T_{stg} , T_J	-55 to 150		$^\circ C$
Thermal resistance, junction-case	$R_{\theta JC}$	7.4	2.3	$^\circ C/W$
Thermal resistance, junction-ambient ⁵⁾	$R_{\theta JA}$	62	62	$^\circ C/W$

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N-Electrical Characteristics at $T_j=25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
BVDSS	Drain-source breakdown voltage	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$	100			V
VGS(th)	Gate threshold voltage	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$	1.0	1.7	3.0	V
RDS(ON)	Drain-source on-state resistance	$V_{GS}=10\text{ V}$, $I_D=5\text{ A}$		55	75	m Ω
RDS(ON)	Drain-source on-state resistance	$V_{GS}=4.5\text{ V}$, $I_D=3\text{ A}$		112	300	m Ω
IGSS	Gate-source leakage current	$V_{GS}=\pm 20\text{ V}$			± 100	nA
IDSS	Drain-source leakage current	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$			200	nA
Ciss	Input capacitance	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$		429.4		pF
Coss	Output capacitance			58.3		pF
Crss	Reverse transfer capacitance			2.9		pF
td(on)	Turn-on delay time	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $R_G=2\text{ }\Omega$, $I_D=5\text{ A}$		15.6		ns
t _r	Rise time			4.2		ns
td(off)	Turn-off delay time			26.8		ns
t _f	Fall time			3.6		ns
Q _g	Total gate charge	$I_D=5\text{ A}$, $V_{DS}=50\text{ V}$, $V_{GS}=10\text{ V}$		7.6		nC
Q _{gs}	Gate-source charge			1.4		nC
Q _{gd}	Gate-drain charge			2.4		nC
V _{plateau}	Gate plateau voltage			4.5		V
I _s	Diode forward current	$V_{GS}<V_{th}$			15	A
ISP	Pulsed source current				45	A
VSD	Diode forward voltage	$I_S=7\text{ A}$, $V_{GS}=0\text{ V}$			1.3	V
trr	Reverse recovery time	$I_S=5\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$		36.1		ns
Q _{rr}	Reverse recovery charge			50.4		nC
I _{rrm}	Peak reverse recovery current			2.6		A

Note

- 1、Calculated continuous current based on maximum allowable junction temperature.
- 2、Repetitive rating; pulse width limited by max. junction temperature.
- 3、Pd is based on max. junction temperature, using junction-case thermal resistance.
- 4、 $V_{DD}=50\text{ V}$, $R_G=50\text{ }\Omega$, $L=0.3\text{ mH}$, starting $T_j=25\text{ }^{\circ}\text{C}$.
- 5、The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^{\circ}\text{C}$.

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P-Electrical Characteristics at $T_j=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-to-Source breakdown voltage	$V_{GS} = 0V, I_D = -250\mu A$	-100	—	—	V
R _{DS(on)}	Static Drain-to-Source on-resistance	$V_{GS}=-10V, I_D=-5A$	—	170	210	mΩ
		$V_{GS}=-4.5V, I_D=-2A$	—	190	230	
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	—	-3	V
I _{DSS}	Drain-to-Source leakage current	$V_{DS} = -100V, V_{GS} = 0V$	—	—	-1	μA
I _{GSS}	Gate-to-Source forward leakage	$V_{GS} = 30V$	—	—	100	nA
		$V_{GS} = -30V$	—	—	-100	
Q _g	Total gate charge	$I_D = -5A, V_{DS}=-80V, V_{GS} = -10V$	—	20	—	nC
Q _{gs}	Gate-to-Source charge		—	3.5	—	
Q _{gd}	Gate-to-Drain("Miller") charge		—	4.6	—	
t _{d(on)}	Turn-on delay time	$V_{GS}=-10V, V_{DS}=-50V, R_{GEN}=25\Omega, I_D=-5A$	—	18	—	ns
t _r	Rise time		—	8	—	
t _{d(off)}	Turn-Off delay time		—	100	—	
t _f	Fall time		—	30	—	
C _{iss}	Input capacitance	$V_{GS} = 0V, V_{DS} = -25V, f = 1MHz$	—	1419	—	pF
C _{oss}	Output capacitance		—	89	—	
C _{rss}	Reverse transfer capacitance		—	45	—	
I _S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode.	—	—	-10	A
I _{SM}	Pulsed Source Current (Body Diode)		—	—	-20	A
V _{SD}	Diode Forward Voltage	$I_S=-1A, V_{GS}=0V$	—	—	-1.2	V
t _{rr}	Reverse Recovery Time	$T_J = 25^\circ\text{C}, I_F = -5A, di/dt = 100A/\mu s$	—	27	—	nS
Q _{rr}	Reverse Recovery Charge		—	24	—	nC

Notes:

- 1、Calculated continuous current based on maximum allowable junction temperature.
- 2、Repetitive rating; pulse width limited by max. junction temperature.
- 3、The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- 4、The value of R_{θJA} is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C

N-Electrical Characteristics Diagrams

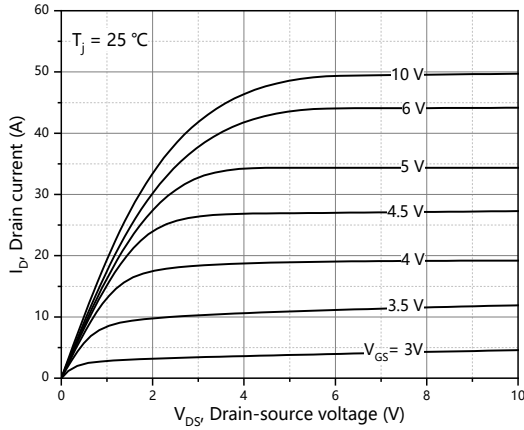


Figure 1, Typ. output characteristics

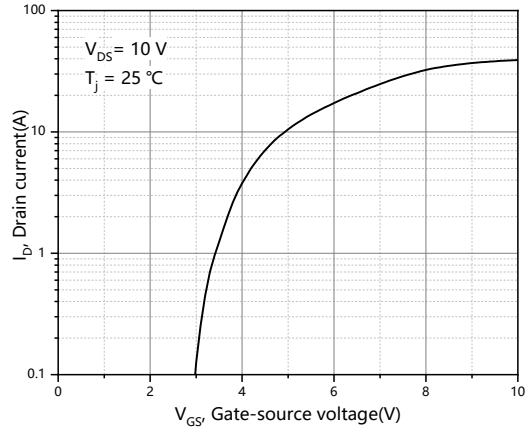


Figure 2, Typ. transfer characteristics

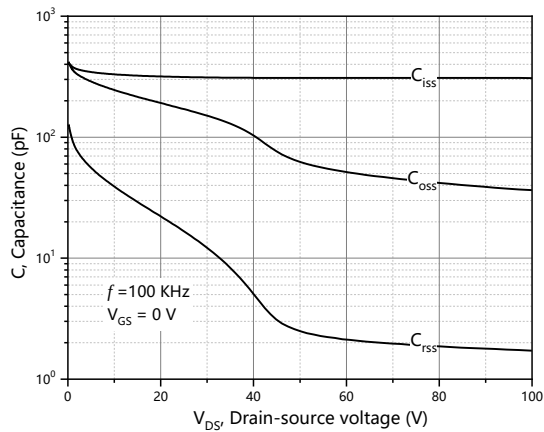


Figure 3, Typ. capacitances

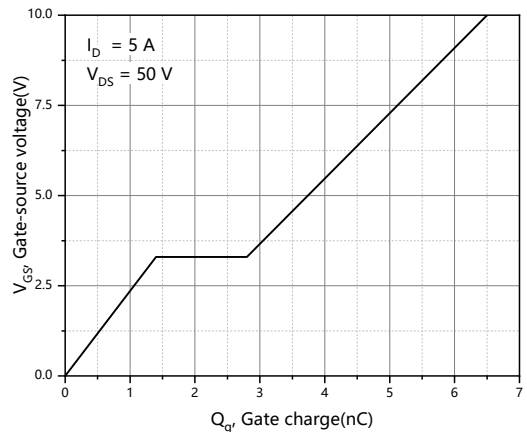


Figure 4, Typ. gate charge

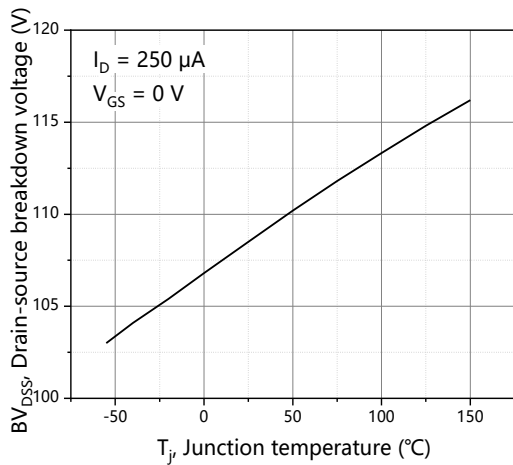


Figure 5, Drain-source breakdown voltage

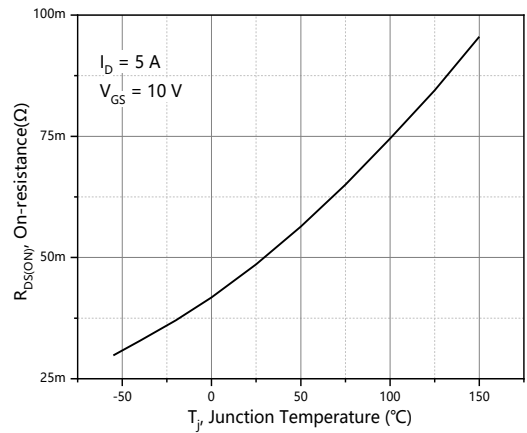


Figure 6, Drain-source on-state resistance

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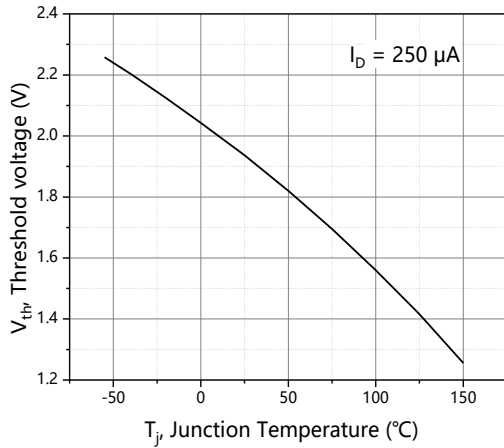


Figure 7, Threshold voltage

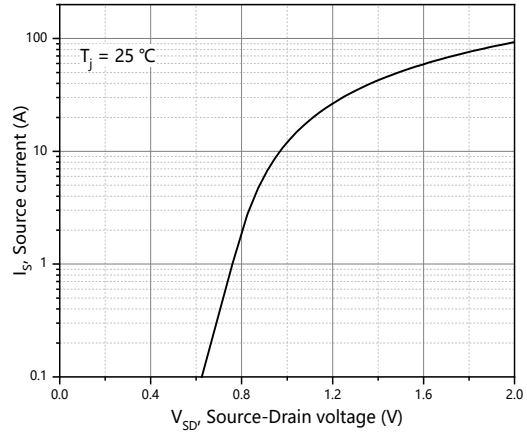


Figure 8, Forward characteristic of body diode

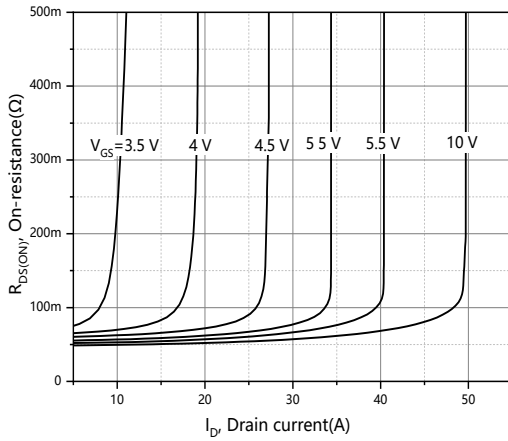


Figure 9, Drain-source on-state resistance

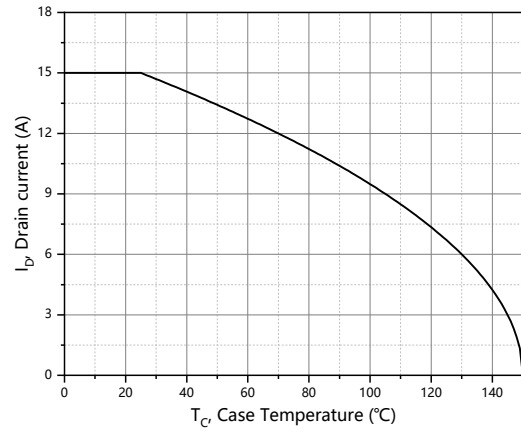


Figure 10, Drain current

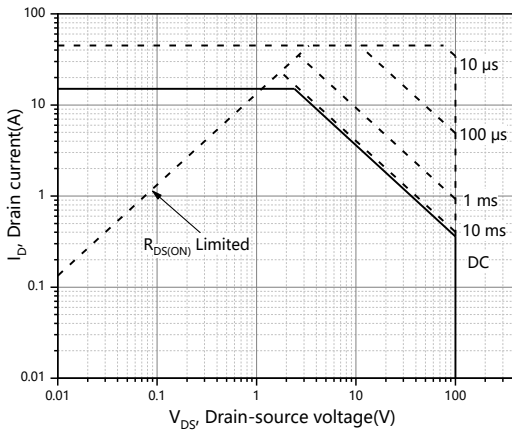


Figure 11, Safe operation area $T_C = 25$ °C

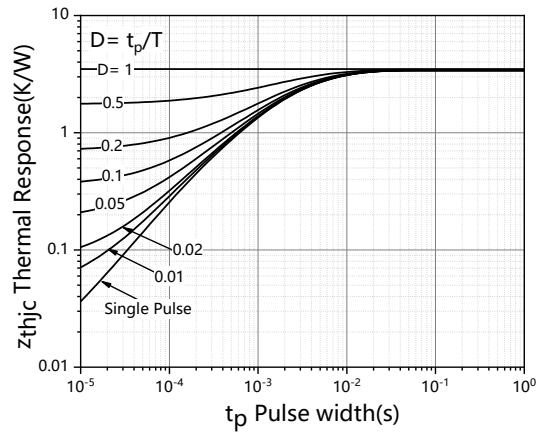


Figure 12, Max. transient thermal impedance

P-Electrical Characteristics Diagrams

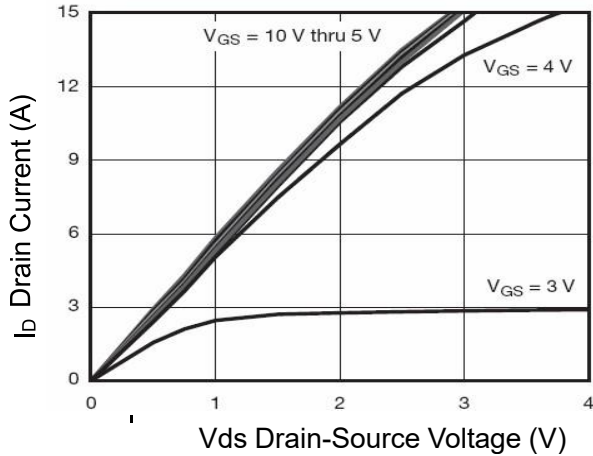


Figure 1 Output Characteristics

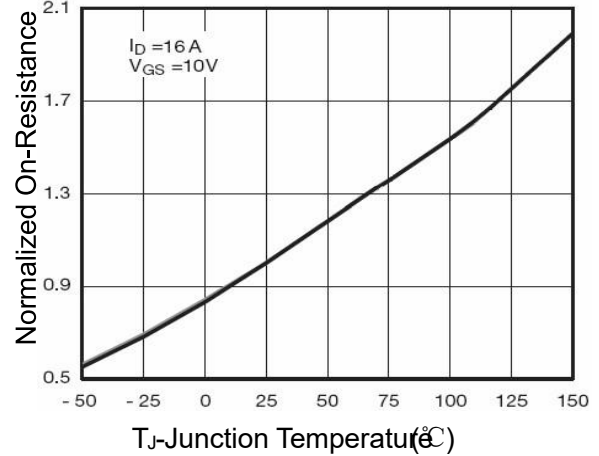


Figure 4 $R_{DS(on)}$ -Junction Temperature

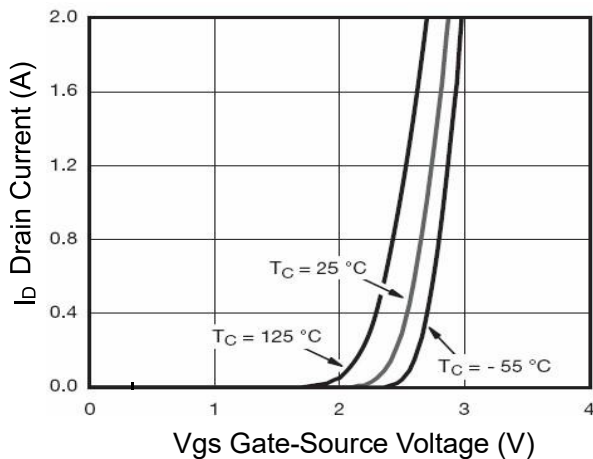


Figure 2 Transfer Characteristics

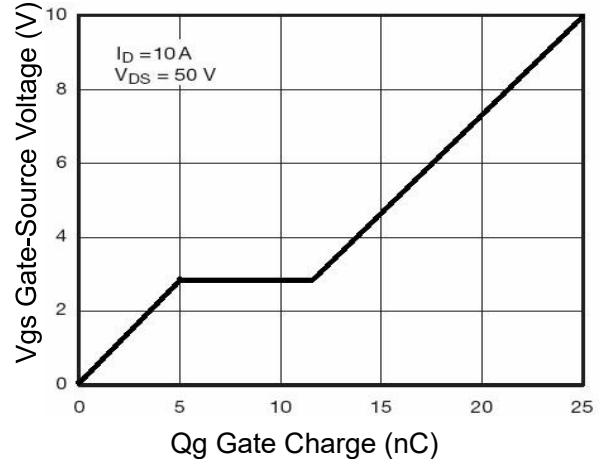


Figure 5 Gate Charge

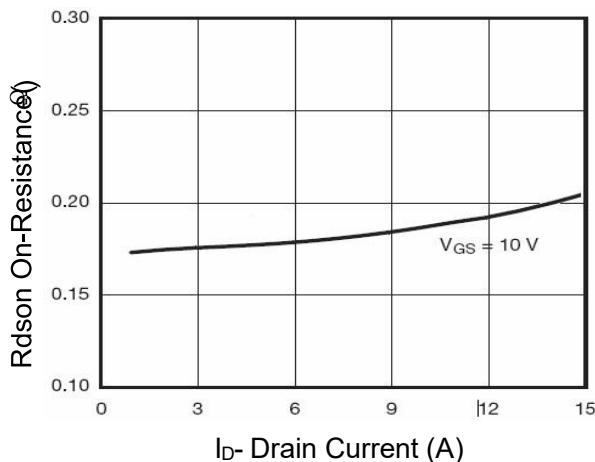


Figure 3 $R_{DS(on)}$ Drain Current

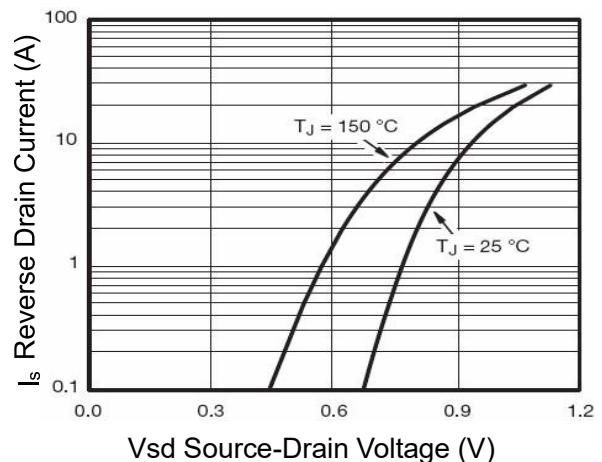


Figure 6 Source- Drain Diode Forward

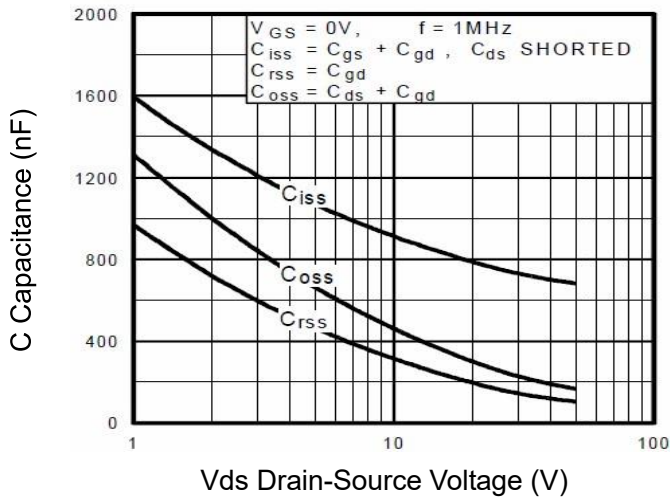


Figure 7 Capacitance vs Vds

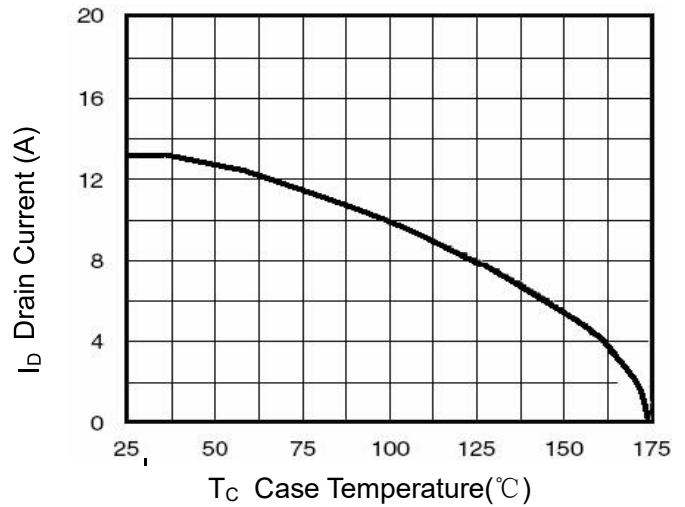


Figure 9 Drain Current vs Case Temperature

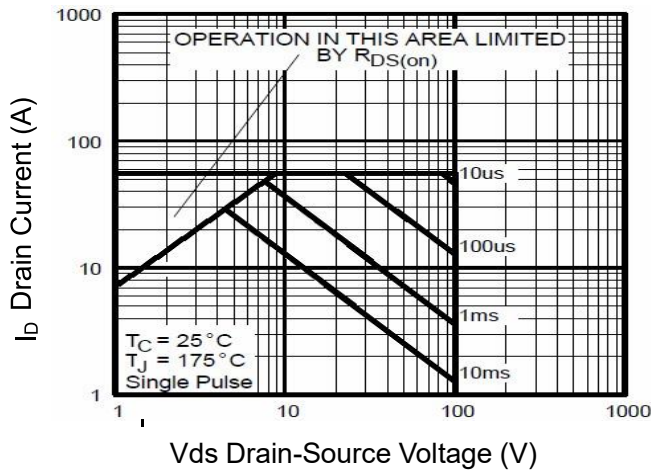


Figure 8 Safe Operation Area

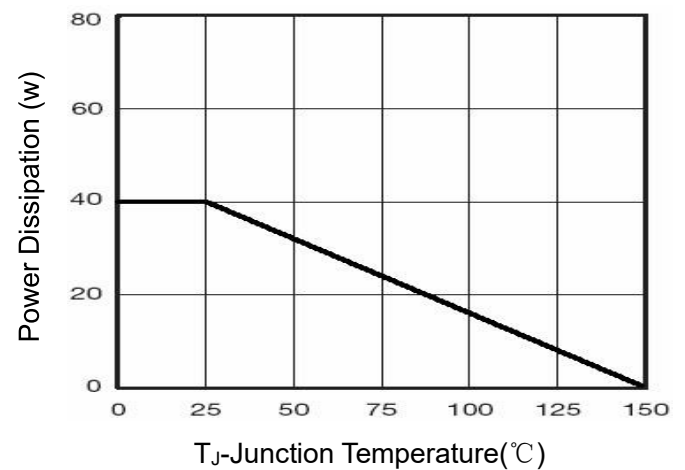


Figure 10 Power De-rating

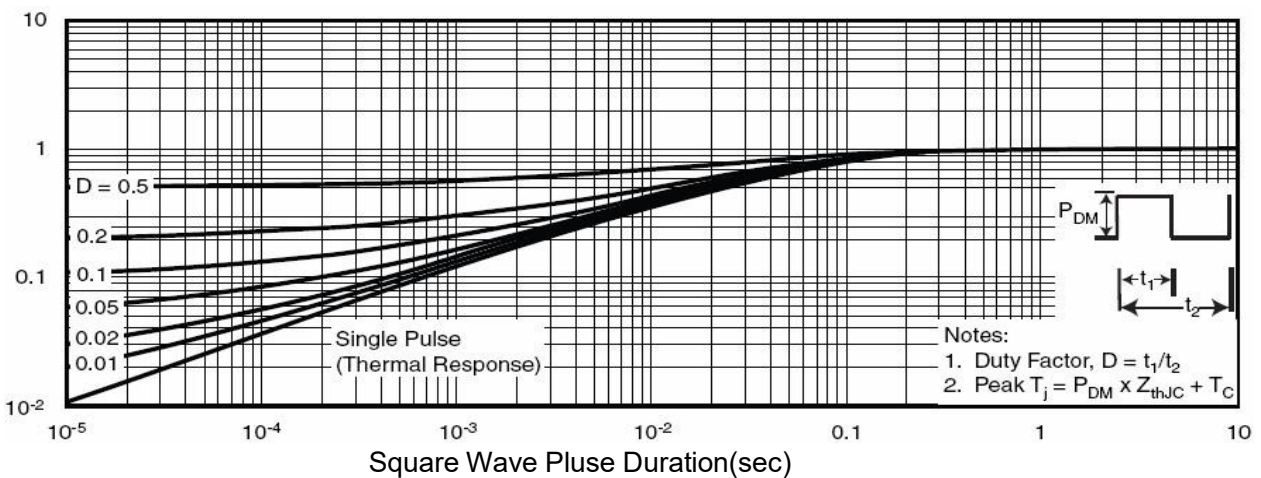
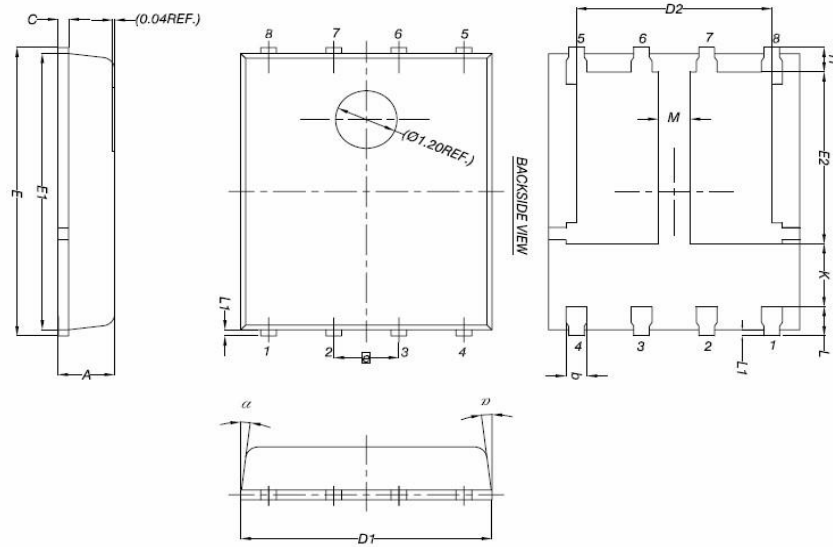


Figure 11 Normalized Maximum Transient Thermal

Package Mechanical Data-DFN5*6-8L-JQ Double



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.66	5.76	5.83
E2	3.37	3.47	3.58
e	1.27BSC		
H	0.41	0.51	0.61
K	1.10	--	--
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	--	--
a	0°	--	12°

100V N+P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
Rve1.0	2019/5/31	Initial release

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