DW9714V

Upgraded Conventional AF Driver IC

FEATURES

120mA output driver with 10-bit resolution DAC
Smart Actuator Control (SAC™) modes
Supply voltage (V_{DD}): 2.3V to 4.3V
I/O voltage (V_{IN}): 1.8V to V_{DD}
Fast mode and Fast mode plus I^2C interface compatible
Power On Reset (POR)
Power Down (PD) mode current consumption less than 1uA
Package: 6-pin WLCSP (0.77mm x 1.14mm x 0.30mm)

APPLICATIONS

Mobile camera
Digital still camera
Camcorder
Web camera
Action camera

GENERAL DESCRIPTION

The DW9714V designed for linear control of Voice Coil Motors (VCM). This device is compatible with DW9714A. The DW9714V has a single 10-bit DAC with 120mA output current sink capability. This device features SAC™ mode which can minimize the mechanical vibration and achieve very fast mechanical settling time. The SAC™ is protected by patent and registered trademark of DONGWOON ANATECH.

The DW9714V operates from a single 2.3V to 4.3V supply. The internal DAC is controlled via an I^2C serial interface that operates at clock rate up to 1MHz. The I^2C address for the DW9714V is 0x18. The DW9714V offers PD mode with current consumption less than 1uA.

The DW9714V can be used for auto focus applications in mobile cameras, digital still cameras, camcorders, web cameras and action cameras.

TYPICAL APPLICATION CIRCUIT

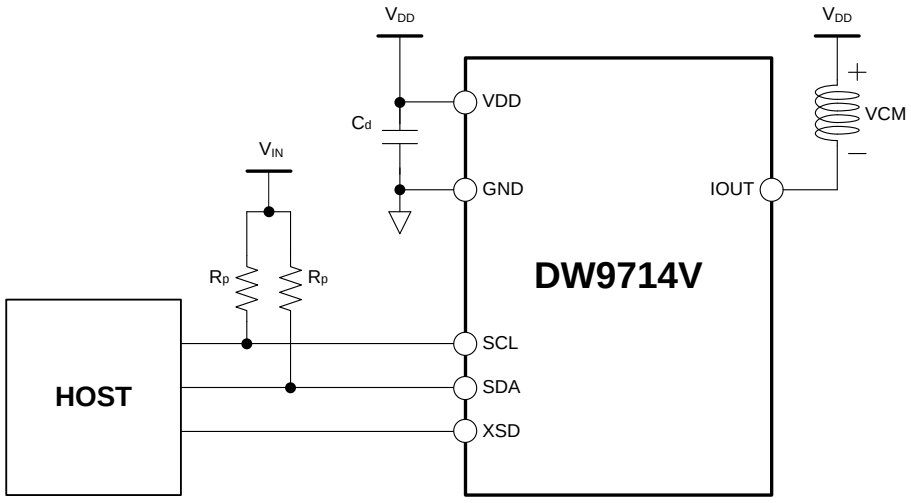

Figure 1. Typical application circuit

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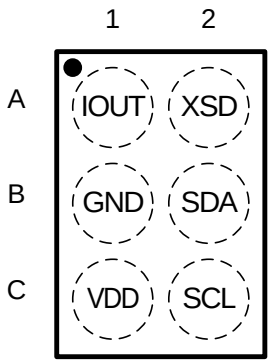
1 Pin Information

1.1 Pin Assignment and Package Dimension



Top View
(Size: 0.77mm X 1.14mm X 0.30mm)

Figure 2. Package dimension

Table 1.

No.	Pin Name	I/O	Description
A1	IOUT	O	Output current sink
A2	XSD	I	Shutdown mode (active low)
B1	GND	-	Ground
B2	SDA	I/O	I^2C interface data input/output
C1	VDD	-	Supply voltage
C2	SCL	I	I^2C interface clock input

2 Block Diagram

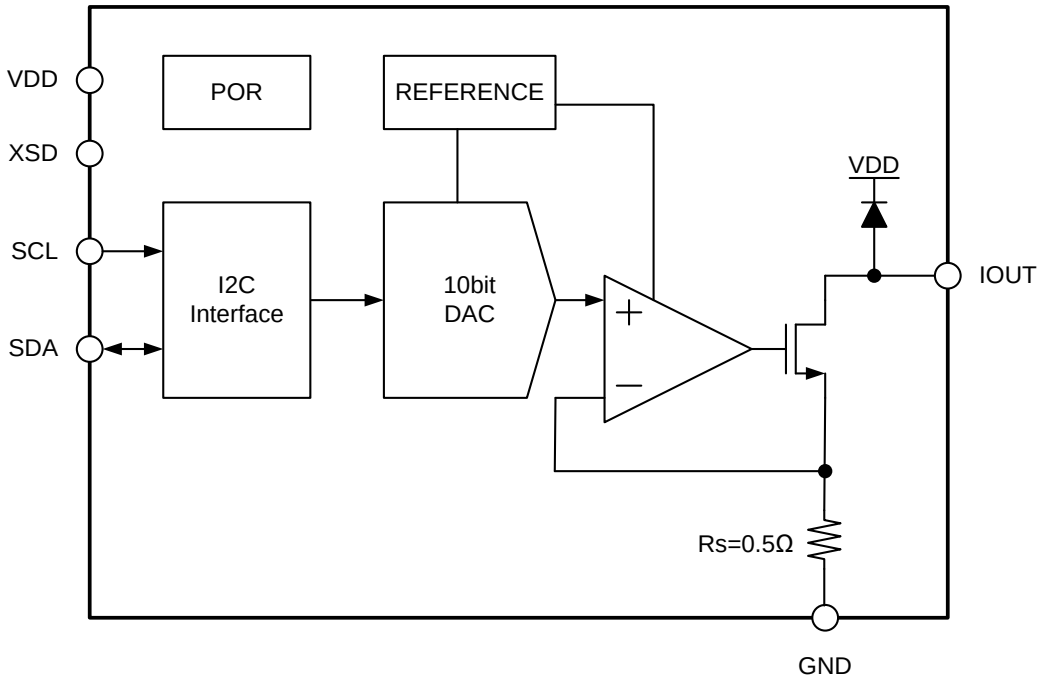


Figure 3. Block Diagram

3 Absolute Maximum Ratings

Table 2.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Power supply voltage	-0.3	5.5	V
V_{IN}	Control input voltage	-0.3	5.5	V
T_{OPR}	Operating temperature range	-40	85	℃
T_J	Junction temperature	-	125	℃
T_{STG}	Storage temperature range	-55	150	℃

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

4 Recommended Operating Condition

Table 3.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Power supply voltage	2.3		4.3	V
V_{IN}	Control input voltage	0		V_{DD}	V
f_{SCL}	Serial clock frequency		400	1000	kHz

5 Electrical Specifications

Table 4. (V_{DD} = 2.8V, V_{IN} = 1.8V, T_A = 25℃, unless otherwise specified)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Overall						
Power supply voltage	V_{DD}		2.3		4.3	V
VDD current	I_{SD}	Shutdown mode (XSD = Low)	-1		+1	uA
	I_{PD}	Power down mode (PD = '1')	-1		+1	uA
	I_Q	Quiescent mode (DAC = 0)			0.35	mA
	I_{ACT}	Operation mode (DAC ≠ 0)			1	mA
Waiting time	t_{OPR}	After V_{DD} rising	1			ms
Logic Input / Output (XSD)						
Input current		V_{IN} = 4.3V	-1		+1	uA
Low level input voltage	V_{IL}	V_{DD} = 2.8V			0.54	V
High level input voltage	V_{IH}	V_{DD} = 2.8V	1.26			V
Logic Input / Output (SCL, SDA)						
Input current		V_{IN} = 3.3V	-1		+1	uA
Low level input voltage	V_{IL}				0.54	V
High level input voltage	V_{IH}		1.26			V
Glitch rejection(1)			50			ns
SDA low level output voltage	V_{OL}	Sink current = 3mA			0.4	V
VCM Driver						
Current resolution				10		bits
INL(1)(2)	I_{INL}				±4	LSB
DNL(1)(2)	I_{DNL}				±1	LSB
Total output resistance(1)		Output current = 100mA			1.5	Ω
Maximum output current	I_{MAX}(3)		115	120	125	mA
Output current	I_{OUTPD}	Power down mode (PD = '1')	-1		1	uA

(1) These are guaranteed by design and characterization.
(2) Linearity is guaranteed for 32code through 992code.
(3) Max operation current = VDD/(Actuator Coil resistance + Total output resistance)
The max operation current can not exceed the Max. output current

6 I²C Protocol

6.1 Start and Stop Condition

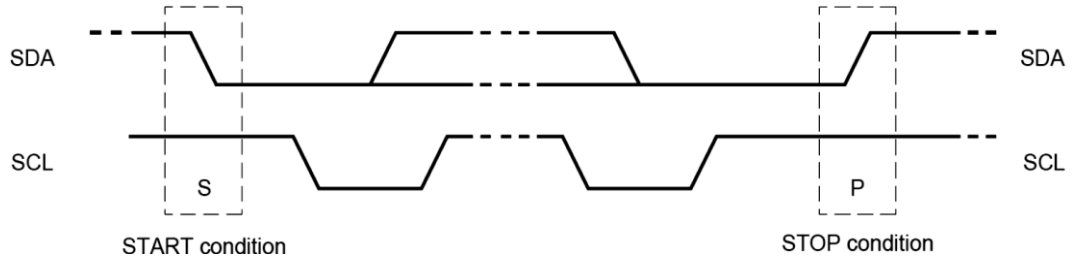


Figure 4. I²C Start and Stop Condition

Within the procedure of the I²C-bus, unique situations arise and are defined as START (S) and STOP (P) conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one of such unique cases. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

6.2 I²C Data Transfer

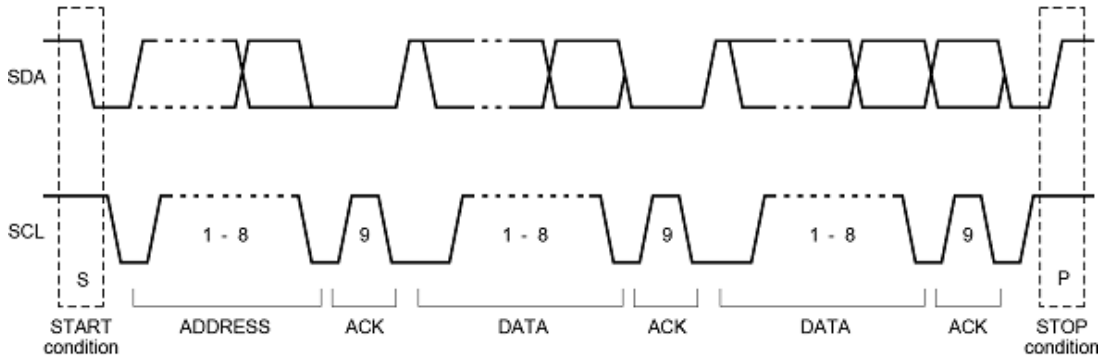


Figure 5. I²C Data transfer

Data transfers follow the above format. After the START condition (S), a slave address is sent. A data transfer is always terminated by a STOP condition (P) generated by the master. However, if the master still needs to communicate on the bus, it can generate a repeated data transfer.

6.3 I²C Timing

Table 5.

Parameter	Symbol	Fast-mode		Fast-mode Plus		Unit
		Min.	Max.	Min.	Max.	
Serial clock frequency	f_{SCL}		400		1000	kHz
Hold time (repeated) START condition.	$t_{HD;STA}$	0.6	-	0.26	-	us
Low period of the SCL clock	t_{LOW}	1.3	-	0.5	-	us
High period of the SCL clock	t_{HIGH}	0.6	-	0.26	-	us
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	0.26	-	us
Data hold time	$t_{HD;DAT}$(1)	0	-	0	-	us
Data set-up time	$t_{SU;DAT}$	100	-	50	-	ns
Rise time of both SDA and SCL signals	t_r	20+0.1C_b(2)	300	20+0.1C_b(2)	120	ns
Fall time of both SDA and SCL signals	t_f	20+0.1C_b(2)	300	20+0.1C_b(2)	120	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	0.26	-	us
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	0.5	-	us
Capacitive load for each bus line	C_b	-	400	-	550	pF
Pulse width of spike suppress	t_{SP}	0	50	0	50	ns
Data valid time(3)	$t_{VD;DAT}$	-	0.9	-	0.45	us
Data valid acknowledge time(4)	$t_{VD;ACK}$	-	0.9	-	0.45	us
Noise margin at the LOW level	V_{nL}	0.1V_{DD}	-	0.1V_{DD}		V
Noise margin at the HIGH level	V_{nH}	0.2V_{DD}	-	0.2V_{DD}		V

(1) A master device must provide a hold time of at least 300ns for the SDA signal (with respect to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL. The maximum data hold time ($t_{HD;DAT}$) has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
(2) C_b is the total capacitance of one bus line in pF. t_r and t_f are measured between 0.3xV_{DD} and 0.7xV_{DD}.
(3) $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
(4) $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

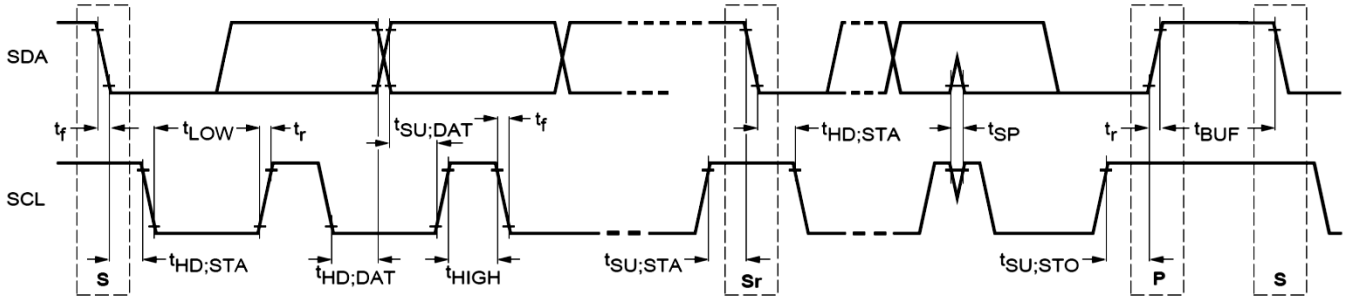


Figure 6. I²C Timing Diagram

7 Operation Mode

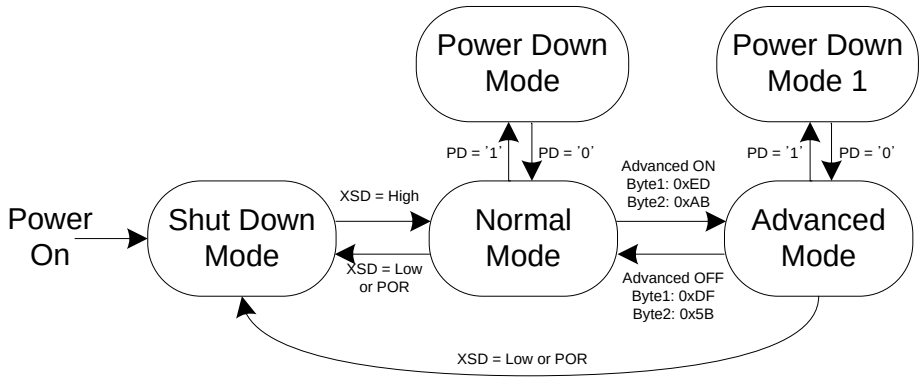


Figure 7. Operation Mode

8 Power Up and Down Sequence

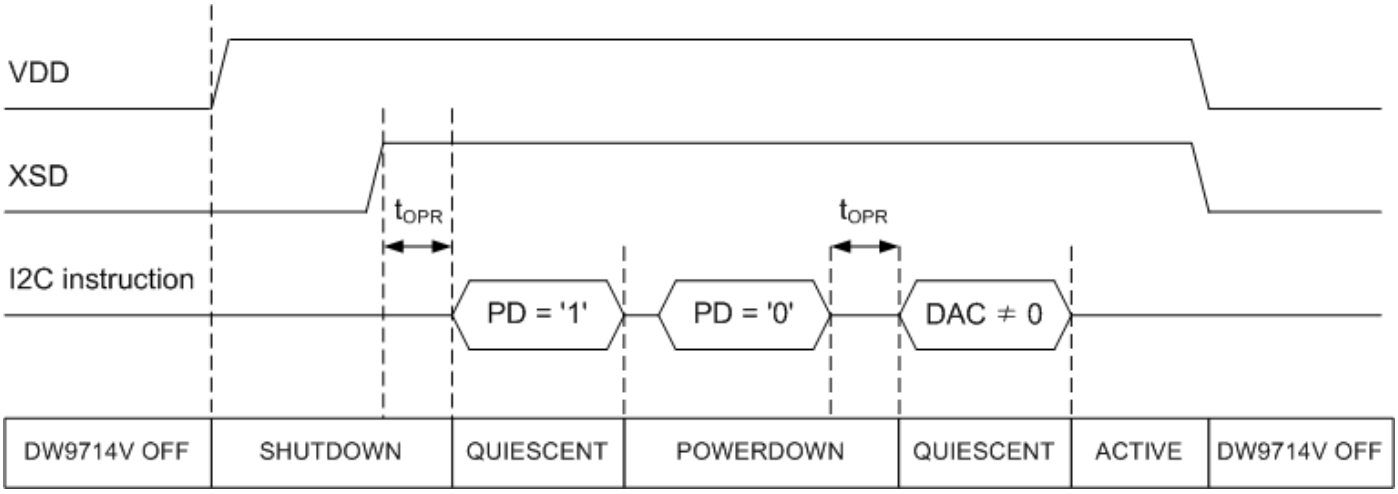


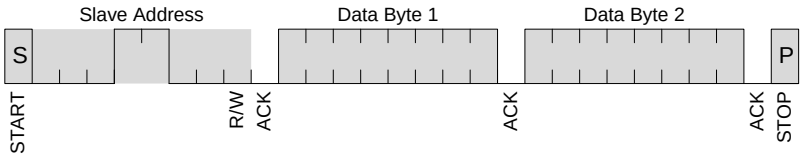
Figure 8. Power Up and Down Sequence

※ The sequence of PD = '1' and PD = '0' must be executed after XSD rising.
※ Waiting time (t_{OPR}) is needed after XSD rising or PD = '0'.
※ XSD must be controlled to "High" or "Low" level. The floating state is not permitted.
※ XSD can be connected to VDD.

9 Normal Mode

9.1 I²C Format

■ **Write Operation**



■ **Read Operation**

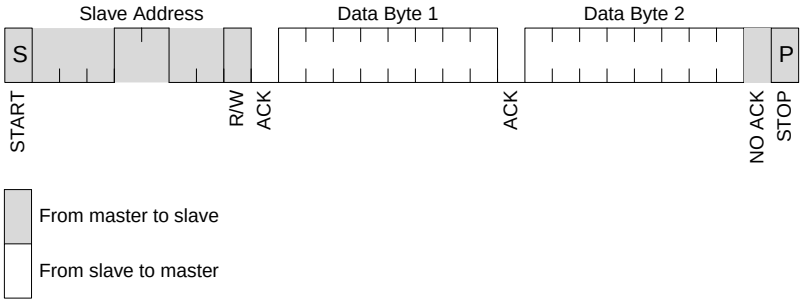


Figure 9. Normal Mode I²C Format

9.2 Register Format

Table 6.

Byte1								Byte2							
PD	FLAG	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	S3	S2	S1	S0

PD: Power down mode

0: Normal operation mode

1: Power down mode (active high)

FLAG: FLAG bit must be checked '0' before Data input **(**D[9:0]**)** registers are written.

During LSC or DLC operation, FLAG bit keeps '1'.

While FLAG = '1', the I^2C command is ignored.

D[9:0]: Data input

Output current = D[9:0] X (120mA / 1023)

S[3:2]: Codes per step

Table 7.

S[3:2]	Codes per step
00	0 (no SRC) – direct driving
01	1
10	2
11	4

S[1:0]: Step period

Table 8.

S[1:0]	Step period [us]
00	Refer to "LSC time table"
01	Refer to "LSC time table"
10	Refer to "LSC time table"
11	Refer to "LSC time table"

9.3 Slew Rate Control Set up Method

9.3.1 Driving mode – Direct, Linear Slope Control (LSC), Dual Level Control (DLC)

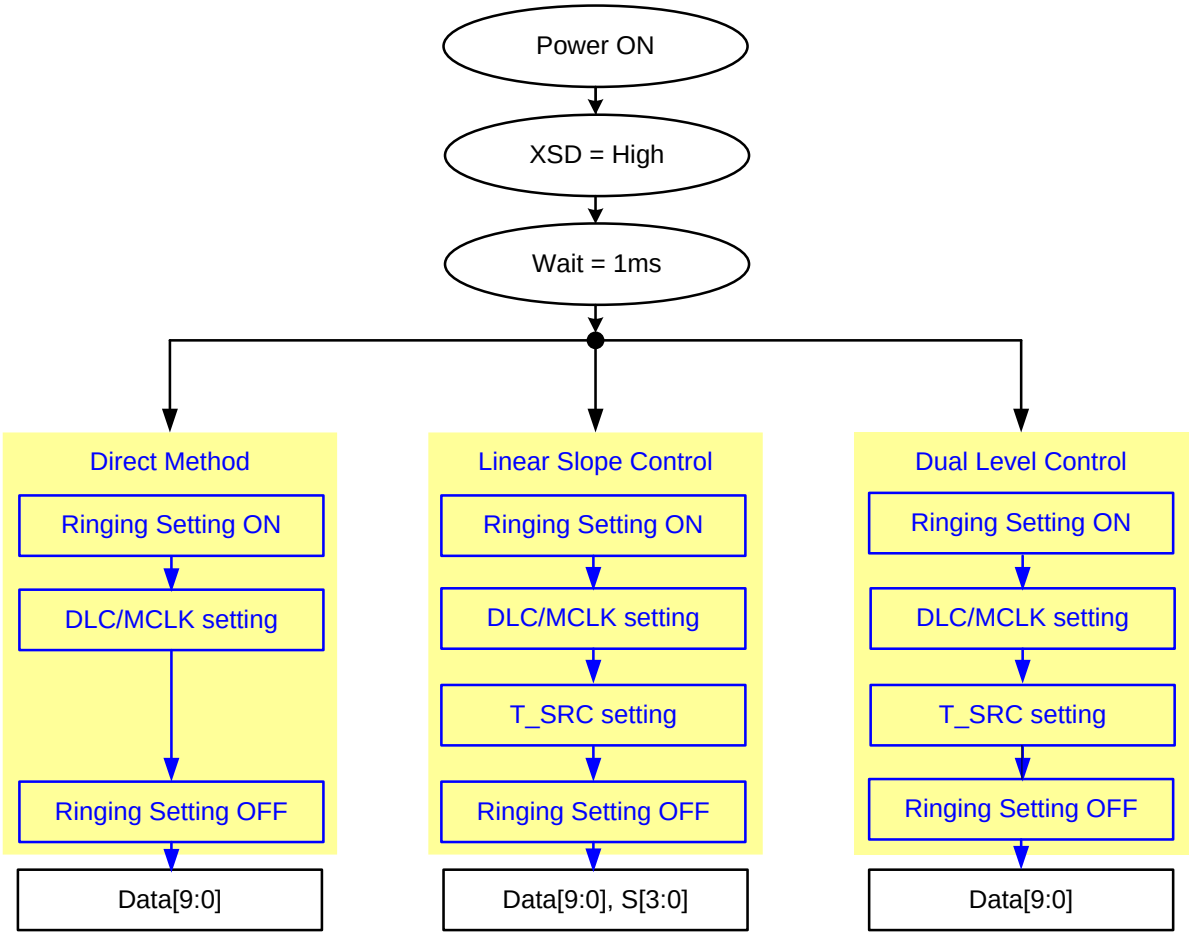


Figure 10. Driving Mode Set up Method

※ When use direct mode after power on, it doesn't need register set.

※ During a driving mode setting sequence, DAC command does not update.

9.3.2 Direct mode set up method

■ Ringing setting ON

Table 9.

Byte1 (0xEC)								Byte2 (0xA3)							
1	1	1	0	1	1	0	0	1	0	1	0	0	0	1	1

■ DLC and MCLK[1:0] setting

Table 10.

Byte1 (0xA1)								Byte2 (default = 0x05)							
1	0	1	0	0	0	0	1	0	0	0	0	DLC	1	MCLK1	MCLK0

DLC: Dual level control mode

0: Direct and LSC

1: DLC mode

MCLK[1:0]

00: x2 (double) 01: x1 (default)

10: half 11: quarter

■ T_SRC[4:0] setting

Table 11.

Byte1 (0xF2)								Byte2 (default = 0x00)							
1	1	1	1	0	0	1	0	T_SRC4	T_SRC3	T_SRC2	T_SRC1	T_SRC0	0	0	0

■ Ringing setting OFF

Table 12.

Byte1 (0xDC)								Byte2 (0x51)							
1	1	0	1	1	1	0	0	0	1	0	1	0	0	0	1

9.3.3 LSC set up method

■ Ringing setting ON

Table 13.

Byte1 (0xEC)								Byte2 (0xA3)							
1	1	1	0	1	1	0	0	1	0	1	0	0	0	1	1

■ DLC and MCLK[1:0] setting

Table 14.

Byte1 (0xA1)								Byte2 (default = 0x05)							
1	0	1	0	0	0	0	1	0	0	0	0	DLC	1	MCLK1	MCLK0

DLC: Dual level control mode

0: Direct and LSC

1: DLC mode

MCLK[1:0]

00: x2 (double) 01: x1 (default)

10: half 11: quarter

■ T_SRC[4:0] setting

Table 15.

Byte1 (0xF2)								Byte2 (default = 0x00)							
1	1	1	1	0	0	1	0	T_SRC4	T_SRC3	T_SRC2	T_SRC1	T_SRC0	0	0	0

■ Ringing setting OFF

Table 16.

Byte1 (0xDC)								Byte2 (0x51)							
1	1	0	1	1	1	0	0	0	1	0	1	0	0	0	1

※ During a SRC setting sequence, DAC command does not update.

■ LSC time table

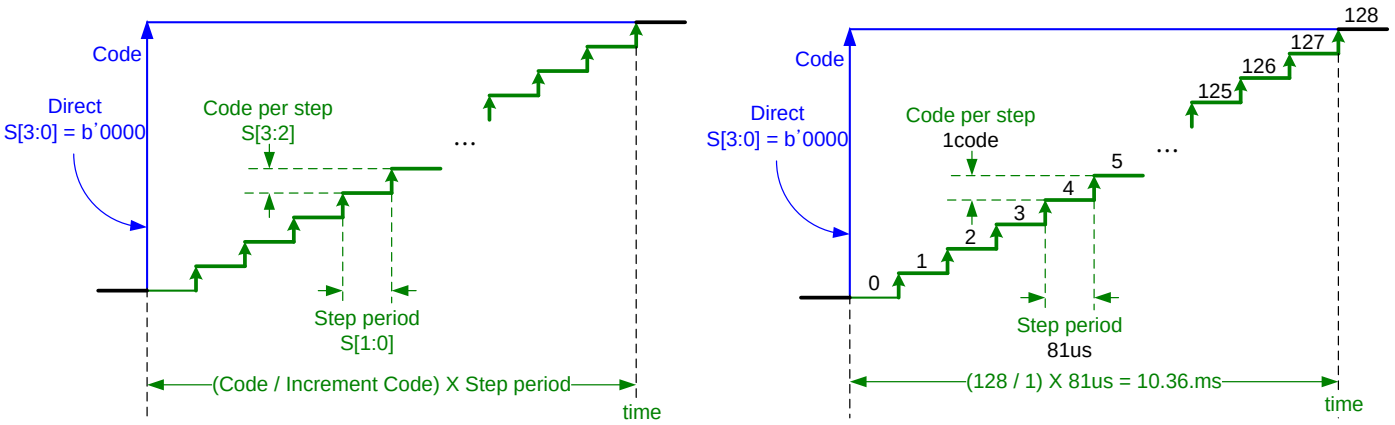
LSC step period is set by S[1:0] and T_SRC[4:0]

Table 17.

Unit: [us]

1 Step period				
T_SRC[4:0]	S[1:0]			
	00	01	10	11
10000	136.0	272.0	544.0	1088.0
10001	130.0	260.0	520.0	1040.0
10010	125.0	250.0	500.0	1000.0
10011	120.0	240.0	480.0	960.0
10100	116.0	232.0	464.0	928.0
10101	112.0	224.0	448.0	896.0
10110	108.0	216.0	432.0	864.0
10111	104.0	208.0	416.0	832.0
11000	101.0	202.0	404.0	808.0
11001	98.0	196.0	392.0	784.0
11010	95.0	190.0	380.0	760.0
11011	92.0	184.0	368.0	736.0
11100	89.0	178.0	356.0	712.0
11101	87.0	174.0	348.0	696.0
11110	85.0	170.0	340.0	680.0
11111	83.0	166.0	332.0	664.0
00000	81.0(default)	162.0	324.0	648.0
00001	79.0	158.0	316.0	632.0
00010	77.5	155.0	310.0	620.0
00011	76.0	152.0	304.0	608.0
00100	74.5	149.0	298.0	596.0
00101	73.0	146.0	292.0	584.0
00110	71.5	143.0	286.0	572.0
00111	70.0	140.0	280.0	560.0
01000	69.0	138.0	276.0	552.0
01001	68.0	136.0	272.0	544.0
01010	67.0	134.0	268.0	536.0
01011	66.0	132.0	264.0	528.0
01100	65.5	131.0	262.0	524.0
01101	65.0	130.0	260.0	520.0
01110	64.5	129.0	258.0	516.0
01111	64.0	128.0	256.0	512.0

■ LSC Scheme



※ 1 step period: Step period S[1:0] = b'00, T_SRC[4:0] = b'0000, Code per step S[3:2] = b'01

Figure 11. LSC Scheme

9.3.4 DLC set up method

■ Ringing setting ON

Table 18.

Byte1 (0xEC)								Byte2 (0xA3)							
1	1	1	0	1	1	0	0	1	0	1	0	0	0	1	1

■ DLC and MCLK[1:0] setting

Table 19.

Byte1 (0xA1)								Byte2 (default = 0x05)							
1	0	1	0	0	0	0	1	0	0	0	0	DLC	1	MCLK1	MCLK0

DLC: Dual level control mode

0: Direct and LSC

1: DLC mode

MCLK[1:0]

00: x2 (double) 01: x1 (default)

10: half 11: quarter

■ T_SRC[4:0] setting

Table 20.

Byte1 (0xF2)								Byte2 (default = 0x00)							
1	1	1	1	0	0	1	0	T_SRC4	T_SRC3	T_SRC2	T_SRC1	T_SRC0	0	0	0

■ Ringing setting OFF

Table 21.

Byte1 (0xDC)								Byte2 (0x51)							
1	1	0	1	1	1	0	0	0	1	0	1	0	0	0	1

※ During a SRC setting sequence, DAC command does not update.

■ DLC time table

Table 22.

Unit: [ms]

$t_{VIB}/2$				
T_SRC[4:0]	MCLK[1:0]			
	00	01	10	11
10000	21.25	10.63	5.31	2.66
10001	20.31	10.16	5.08	2.54
10010	19.53	9.77	4.88	2.44
10011	18.75	9.38	4.69	2.34
10100	18.13	9.06	4.53	2.27
10101	17.50	8.75	4.38	2.19
10110	16.88	8.44	4.22	2.11
10111	16.25	8.13	4.06	2.03
11000	15.78	7.89	3.95	1.97
11001	15.31	7.66	3.83	1.91
11010	14.84	7.42	3.71	1.86
11011	14.38	7.19	3.59	1.80
11100	13.91	6.95	3.48	1.74
11101	13.59	6.80	3.40	1.70
11110	13.28	6.64	3.32	1.66
11111	12.97	6.48	3.24	1.62
00000	12.66	6.33 (default)	3.16	1.58
00001	12.34	6.17	3.09	1.54
00010	12.11	6.05	3.03	1.51
00011	11.88	5.94	2.97	1.48
00100	11.64	5.82	2.91	1.46
00101	11.41	5.70	2.85	1.43
00110	11.17	5.59	2.79	1.40
00111	10.94	5.47	2.73	1.37
01000	10.78	5.39	2.70	1.35
01001	10.63	5.31	2.66	1.33
01010	10.47	5.23	2.62	1.31
01011	10.31	5.16	2.58	1.29
01100	10.23	5.12	2.56	1.28
01101	10.16	5.08	2.54	1.27
01110	10.08	5.04	2.52	1.26
01111	10.00	5.00	2.50	1.25

※ Recommended that DLC step period is set $t_{VIB}/2$ (t_{VIB} = VCM vibration period)

9.3.5 SRC Test Results

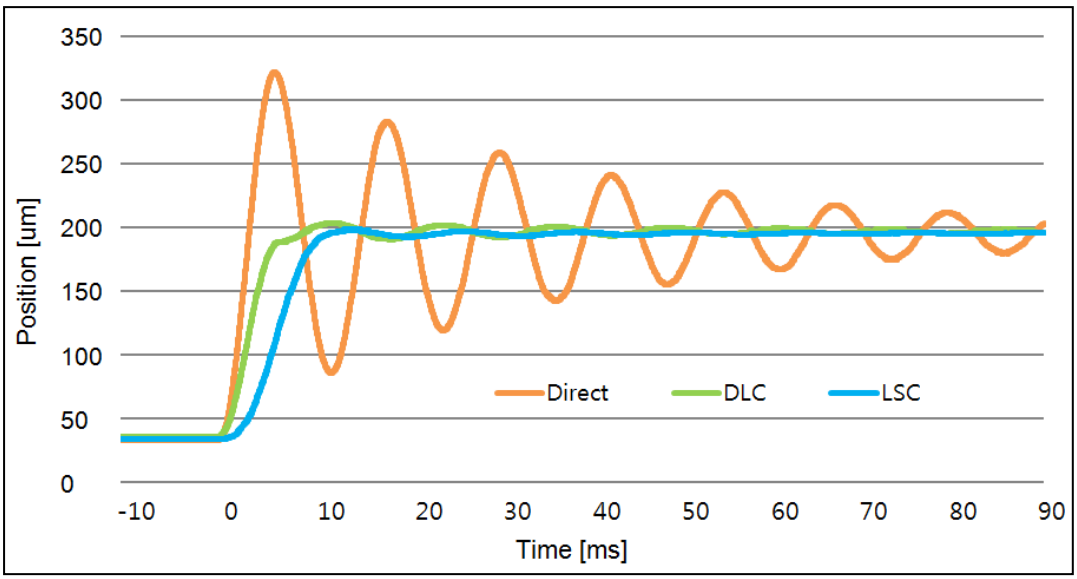


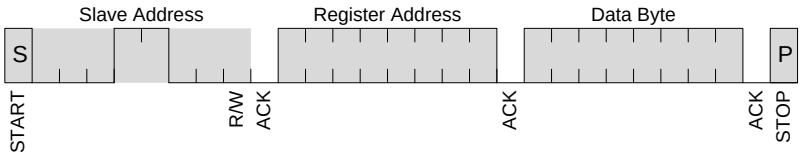
Figure 12. SRC Test Results

10 Advanced Mode

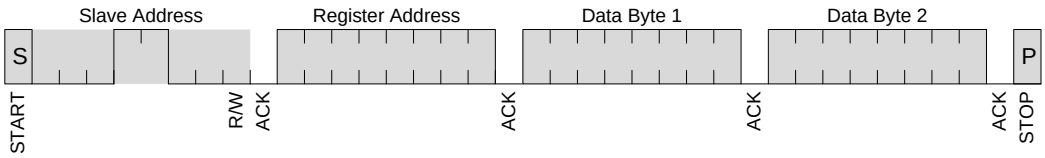
DW9714V is compatible with DW9714A when operating in normal mode. In addition to the normal mode, DW9714V has an advanced mode that includes SAC. It enters its advanced mode by writing 0xED, 0xAB sequentially. When it is in its advanced mode, it can be back to its normal mode by writing 0xDF, 0x5B sequentially. DW9714V supports SAC 2/3/3.5 in its advanced mode.

10.1 I²C Format

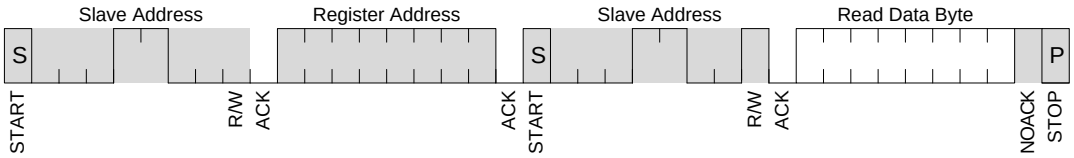
■ Write Operation – Byte Write



■ Write Operation – Sequential Write



■ Read Operation – Selective Read



■ Read Operation – Sequential Read

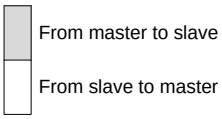


Figure 13. Advanced Mode I²C Format

10.2 Register Map

Table 23.

Name	Addr.	Default	R/W	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
IC INFO	0x00	0xFE	R	IC Manufacturer ID				IC Model			
IC VER.	0x01	-	R					Design Round			
CONTROL	0x02	0x00	R/W								PD
VCM MSB	0x03	0x00	R/W							D9	D8
VCM LSB	0x04	0x00	R/W	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	0x05	0x00	R								BUSY
SAC_CFG	0x06	0x00	R/W	RING_EN	NRC_INFL1	NRC_INFL0	NRC_TIME	SAC_MODE 3	SAC_MODE 2	SAC_MODE 1	SAC_MODE 0
PRESC	0x07	0x00	R/W							PRESC1	PRESC0
SACT	0x08	0x00	R/W		SACT6	SACT5	SACT4	SACT3	SACT2	SACT1	SACT0
PRESET	0x09	0x00	R/W	PRESET7	PRESET6	PRESET5	PRESET4	PRESET3	PRESET2	PRESET1	PRESET0
NRC	0x0A	0x00	W							NRC_EN	NRC_MODE

■ IC Information

Table 24.

Name	Addr.	Default	R/W	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
IC INFO	0x00	0xFE	R	IC Manufacturer ID				IC Model			

■ IC Version

Table 25.

Name	Addr.	Default	R/W	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
IC VER.	0x01	-	R					Design Round			

■ Control

Table 26.

Name	Addr.	Default	R/W	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
CONTROL	0x02	0x00	R/W								PD

PD: Power down mode

0: Normal operation mode

1: Power down mode (active high)

■ VCM MSB & VCM LSB

Table 27.

Name	Addr.	Default	R/W	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
VCM MSB	0x03	0x00	R/W							D9	D8
VCM LSB	0x04	0x00	R/W	D7	D6	D5	D4	D3	D2	D1	D0

※ I_{OUT}(DAC output) is updated when address 0x04 is written.

Output current = D[9:0] X (120mA / 1023)

■ Status

Table 28.

Name	Addr.	Default	R/W	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
STATUS	0x05	0x00	R								BUSY

BUSY: Ringing control operation state check

0: Ringing control ending

1: Ringing control operating

■ SAC configuration

Table 29.

Name	Addr.	Default	R/W	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
SAC_CFG	0x06	0x00	R/W	RING_EN	NRC_INFL1	NRC_INFL0	NRC_TIME	SAC_MODE3	SAC_MODE2	SAC_MODE1	SAC_MODE0

RING_EN: Ringing control enable

0: Direct mode

1: Ringing control (LSC, SAC, SLSC)

NRC_INF[1:0]: Noise Reduction Control (NRC) inflection point

Table 30.

NRC_INF[1:0]	Inflection point
00	25.8%
01	33.8%
10	41.9%
11	50.0%

NRC_TIME: NRC operation time

0: 32.11ms

1: 64.22ms

SAC_MODE[3:0]: Ringing control mode

Table 31.

SAC_MODE[3:0]	Ringing control mode	SAC_MODE[3:0]	Ringing control mode
0000	SAC2	0110	LSC Step 1
0100	SAC3	1010	LSC Step 2
1000	SAC3.5	1110	LSC Step 4
0011	SLSC	else	Reserved

※ LSC Step: code per step

■ SAC t_{VIB}

Table 32.

Name	Addr.	Default	R/W	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
PRESC	0x07	0x00	R/W							PRESC1	PRESC0
SACT	0x08	0x00	R/W		SACT6	SACT5	SACT4	SACT3	SACT2	SACT1	SACT0

PRESC[1:0]: Prescaler (SAC period divider)

Table 33.

PRESC[1:0]	SAC period
00	1
01	2
10	4
11	8

SACT[6:0]: SAC time selection

SAC setting time is set by PRESC[1:0] and SACT[6:0] registers and following below equation.

SAC setting time = t_{VIB} = (3.81ms+(SACT [6:0]) x 0.03ms)) x (PRESC[1:0])

■ Preset

Table 34.

Name	Addr.	Default	R/W	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
PRESET	0x09	0x00	R/W	PRESET7	PRESET6	PRESET5	PRESET4	PRESET3	PRESET2	PRESET1	PRESET0

PRESET[7:0]: NRC current setting

DAC code for preset = { PRESET7, PRESET6,… PRESET1, PRESET0 }

ex) PRESET[7:0] = b'1111 0000 is DAC code for preset = b'1 1110 0000

■ **NRC**

Table 35.

Name	Addr.	Default	R/W	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
NRC	0x0A	0x00	W							NRC_EN	NRC_MODE

NRC_EN: NRC enable

0: Direct mode

1: NRC

NRC_MODE: NRC setting

0: NRC start

1: NRC landing

10.3 Smart Actuator Control (SAC™)

Mechanical ringing is an inherent problem in VCM. SAC™ is a solution for reducing mechanical ringing and achieving very fast settling time, and as a result, enhances autofocus response times, image quality, and user experience.
SAC™ incorporates a wide band of tolerance around the vibration period of the VCM to compensate for manufacturing variability in the mechanical vibration period (t_{VIB}) of VCM.
DW9714V offers various SAC™ modes which are trade-off between operation time and tolerance. User can choose optimal SAC™ mode for each application.

■ SAC setting Time and Tolerance

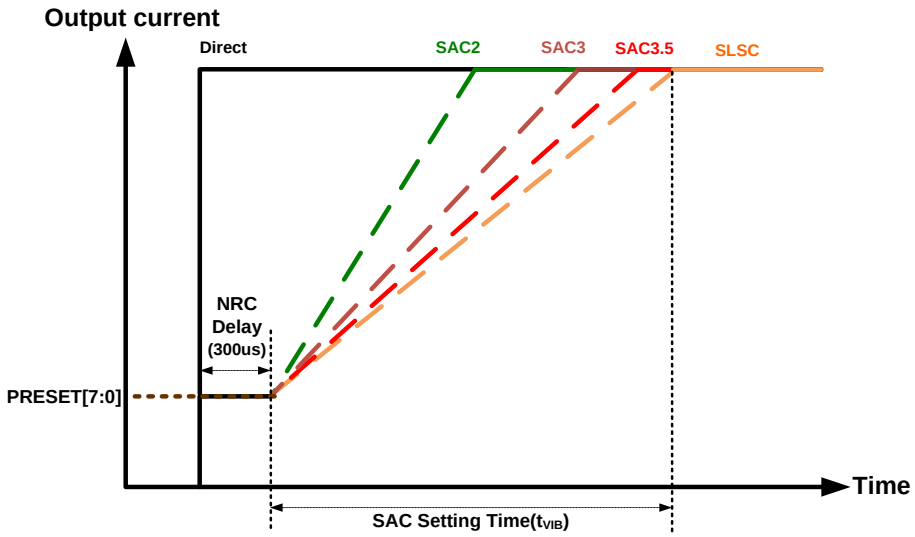


Figure 14. SAC Setting Time

Table 36.

Mode	SAC operation time(1)	Tolerance of VCM(2)
Direct	-	-
SAC2	0.50 x t_{VIB}	± 6 %
SAC3	0.75 x t_{VIB}	± 16%
SAC3.5	0.92 x t_{VIB}	± 24%
SLSC	1.00 x t_{VIB}	± 31%

(1) The time to reach a target current
(2) Tolerance can be changed by mechanical characteristics of specific actuators.

10.4 NRC Start & NRC Landing

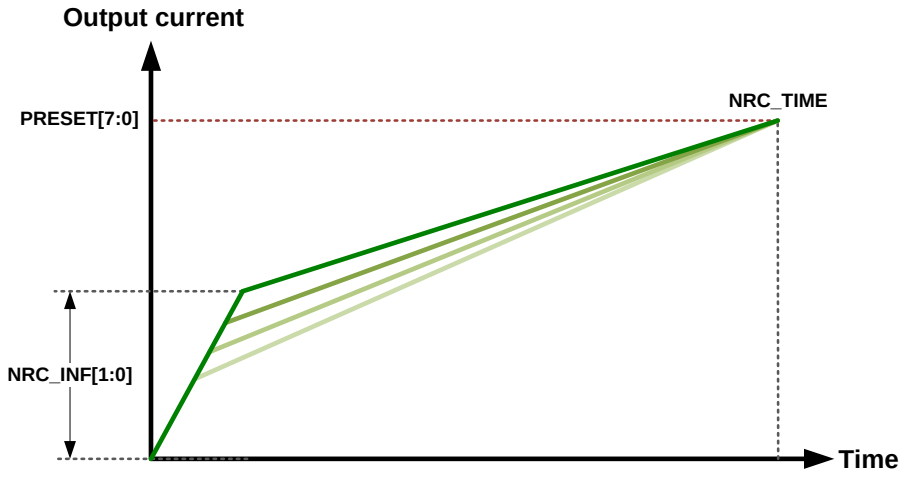


Figure 15. NRC start

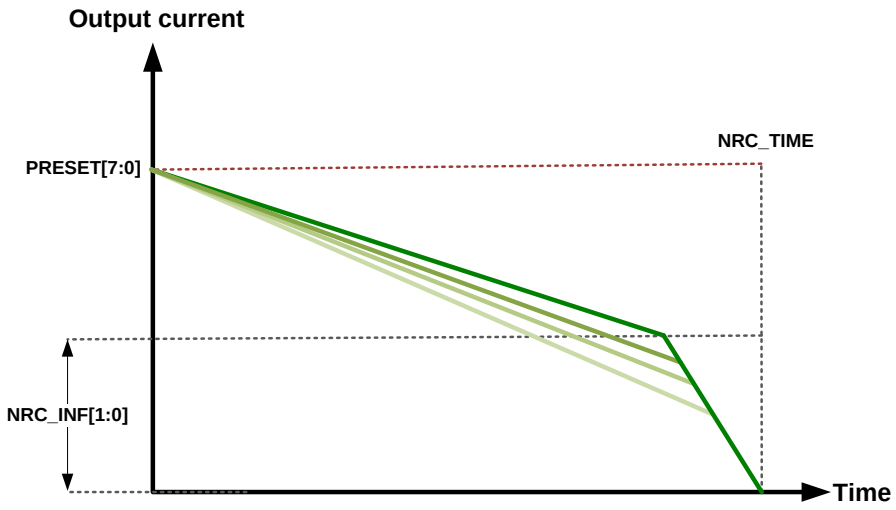


Figure 16. NRC landing

※ The NRC start and NRC landing are modes reducing sound noise level from the used VCM application.

※ The NRC start and NRC landing algorithm is set by PRESET[7:0] and NRC_TIME, NRC_INF[1:0].

※ PRESET[7:0] is NRC current setting.

※ NRC_INF[1:0] is NRC Inflection point setting (25~50%).

11 Typical Application Circuit

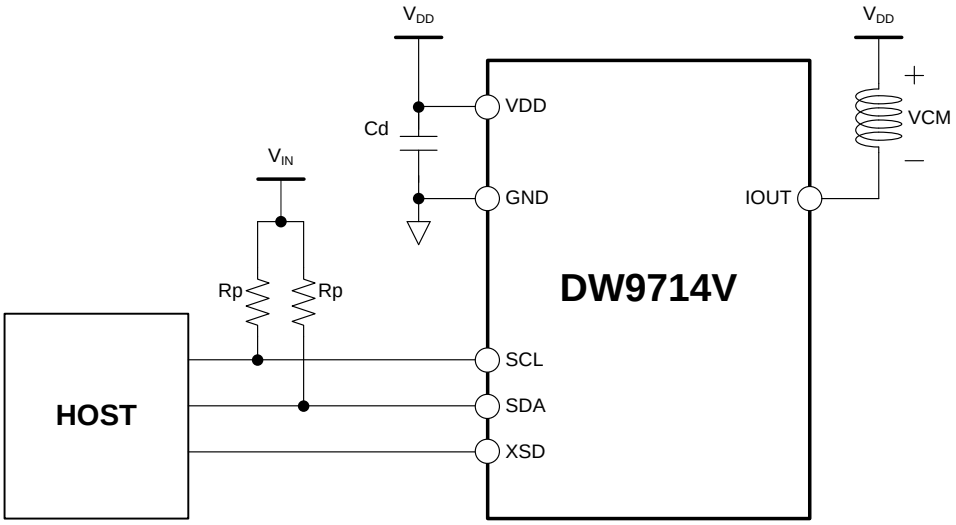
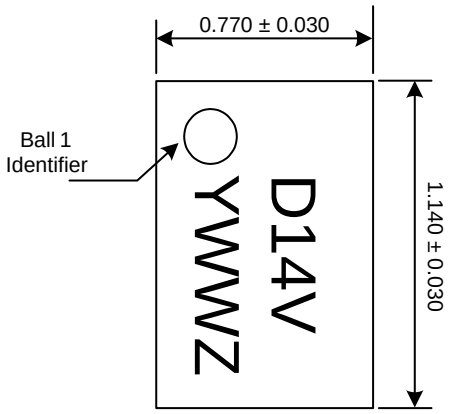


Figure 17. Typical Application Circuit

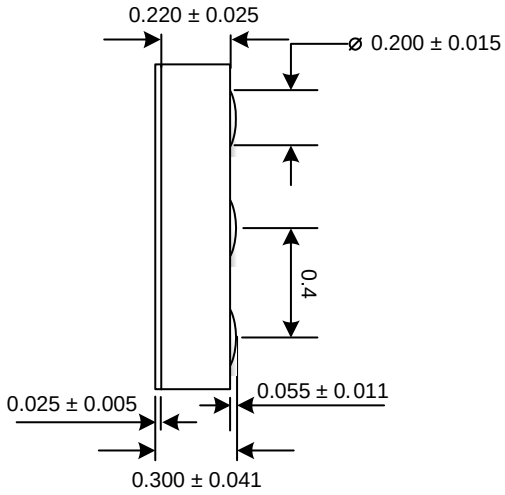
※ Power supply decoupling capacitor (Cd) must be placed as close to the VDD and GND as possible.
※ The value of Cd is recommended more than 1uF.
※ Recommend resistor (Rp) value is 1.2kΩ ~ 4.7kΩ @ (V_{IN} = 1.8V)
※ PCB pattern of VDD, GND and IOUT must be as short and wide as possible.
※ XSD must be controlled by GPIO. Otherwise they can be connected to VDD.

12 Package Dimension

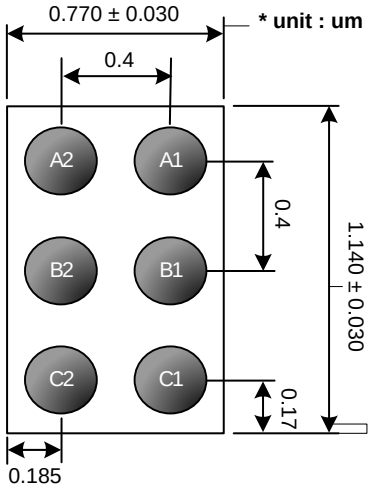


Top View

NO	NAME	I/O
A1	IOUT	O
A2	XSD	I
B1	GND	-
B2	SDA	I/O
C1	VDD	-
C2	SCL	I



Side View



Bottom View

Figure 18. Package Dimension